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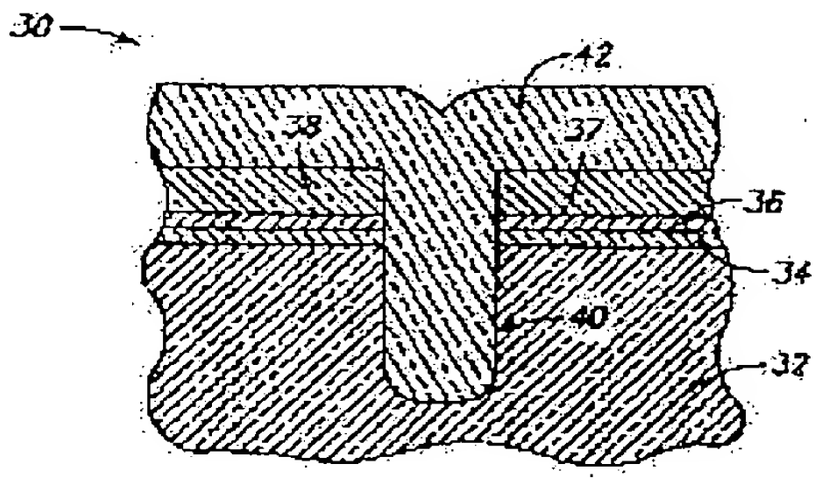
(54) SEMICONDUCTOR PROCESSING METHOD FOR FORMING SUBSTRATE-SEPARATING TRENCH

(57)Abstract:
PURPOSE: To provide a semiconductor processing method for forming a trench which separates a substrate.
CONSTITUTION: This method comprises following steps (a) to (g): (a) a step for providing a first material layer 34 with a selected thickness on a substrate 32, (b) a step for providing a sacrificial layer 38 with a selected thickness on the first material layer 34, (c) a step for patterning and etching the substrate 32 through the first material layer 34 and the sacrificial layer 38, and forming a separating trench, (d) a step for filling the trench by depositing a trench-filling material 42a, having a selected thickness on the substrate and in the trench, (e) a step for planar-etching the trench filling material 42a by using the sacrificial layer 38 as an etch stop, (f) a step for leaving pillars projecting upwards from the substrate top surface by etching the sacrificial layer 38, and (g) a step for selectively etching the pillars to the substrate top surface.



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* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the trench separation approach in semi-conductor processing.
[0002]
[Description of the Prior Art] An integrated circuit is accumulated chemically and physically by substrates, such as a silicon wafer, by carrying out patterning of the field of a substrate, and carrying out patterning of the layer on a substrate. The above-mentioned field and a layer can be made into conductivity, and a conductor and resistance can be manufactured. Moreover, the conductivity of a type which is different in the above-mentioned field and a layer can be given, and this is a transistor and requirements indispensable to manufacture of diode. When forming into a substrate, various circuit elements, i.e., device, it is necessary to separate namely, insulate such a device of each other.
[0003] In case an integrated circuit is manufactured, the various techniques for insulating electrically the device formed into the bulk substrate have been developed. The technique of a certain developed common knowledge omits partial oxidation (LOcal Oxidation of Silicon) of silicon, is called LOCOS separation, and forms the oxide of a half-hollow mold in the non active (or field) field of a substrate in this technique. The principle of the LOCOS method is growing up an oxide into a desired field field alternatively. Growth of such oxide is performed by covering an active field by the film of silicon nitride, and the film of the above-mentioned silicon nitride prevents that oxidation takes place under it. The layer of a nitride exposes up patterning and the silicon field by which it is etched and a field oxide is needed in it, and is grown up. Then, a wafer is exposed on oxidation conditions. An oxidant grows up to be a part without a masking nitride. However, in the periphery section of masking of a nitride, that oxide is spread a little in the side.
[0004] Thereby, an oxide grows under the periphery section of a nitride and this periphery section is raised. The configuration of the oxide of the periphery section of a nitride forms the wedge of the oxide which inclines gently, and this wedge joins the oxide layer of a lower layer pad. The above-mentioned wedge is called the beak (bird's beak) of a bird. It elongates to the side of field oxide and the beak of a bird goes into the active field of a device. One of such the faults of separation technology is producing the field oxide which has the dimension of the longitudinal direction where the beak of the above-mentioned bird is bigger than the lower limit of the photograph function it being used in order to form mask opening in a nitride.
[0005] Therefore, it takes for the geometric configuration of a device to approach a submicron dimension, and the effectiveness of the usual LOCOS separation technology approaches the limitation, and CMOS and the alternative separation process for bipolar techniques are needed. There is trench separation as one of such the techniques. In this technique, it fills up, and the separated trench is perpendicularly arranged in a substrate, and separates namely, insulates the electric device in the both sides of this trench. This invention relates to the art for forming the substrate separation trench like ****.
[0006] The trouble accompanying the technique is explained to a separation trench technical list with the conventional technique with reference to drawing 1 thru/or drawing 5 . Drawing 1 shows

the semi-conductor substrate 10 which consists of a bulk substrate 12, a film 14 of pad oxide, and a layer 16 of a photoresist. Patterning of the photoresist layer 16 will be carried out, it will form the contact opening 20, and the trench which penetrates this will be formed in this opening.

[0007] If drawing 2 is referred to, the pad oxide layer 14 and the bulk substrate 12 will be etched like illustration, and will form dead air space 22, i.e., a trench.
[0008] Reference of drawing 3 is growing up the layer 24 of SiO2 in a trench 22.
[0009] Like illustration, the additional separation implant 26 can also be formed in the base of a trench 22. For example, when the bulk substrate 12 consists of silicon with which the device of n channels will be formed (p-), the implant 26 can be made into the implant (p+) and the electric separation effectiveness, i.e., the insulating effectiveness, can be further brought about between the circuit elements which should be formed in the both sides of a trench 22. Before the implant generally removes the mask layer shown in drawing 1 , it is prepared.
[0010] If drawing 4 is referred to, the layer 28 which consists of a trench packing material would be formed in the crowning of a wafer, and will be filled up with the trench 22. The ingredient of a layer 28 can be used as the polish recon which has ** filled up with the volume of a trench 22, an oxide, or other ingredients. It is not necessary to necessarily make the ingredient of a layer 28 into an insulating material. The reason is that the layer 26 of oxide brings the electric insulating effectiveness to the field of the side of a trench 22. Generally such a layer is deposited in the shape of conformal, and forms the part 30 of a hollow like illustration, i.e., a V character mold.
[0011] If drawing 5 is referred to, a layer 28 will be exposed by proper etching and will be removed to the point of leaving the trench 22 with which it filled up in general. However, generally partial 30a of a V character mold remains like illustration also after etching with the property deposited in the shape of [of a layer 28] conformal, and this is not desirable.
[0012]
[Problem(s) to be Solved by the Invention] It is desirable to improve the above-mentioned technique and other above-mentioned techniques which form a substrate separation trench.
[0013]
[Means for Solving the Problem] According to the description with this invention, the semi-conductor art for forming a substrate separation trench The process which prepares on a substrate the layer which has the selected thickness and consists of the selected ingredient, The process which prepares the sacrifice layer which has the selected thickness and consists of the selected dirty stop ingredient on the layer which consists of the ingredient by which selection was made [above-mentioned], The process which etches into a patterning list into the above-mentioned substrate through the layer which consists of the above-mentioned sacrifice layer and the ingredient by which selection was made [above-mentioned], and forms a separation trench, The process which the upper part list of the above-mentioned substrate is made to deposit the trench packing material which has the selected thickness into the above-mentioned separation trench, and is filled up with the above-mentioned separation trench, The above-mentioned sacrifice layer is etched from the process which carries out flattening etching of the above-mentioned trench packing material, and the above-mentioned substrate, using the above-mentioned sacrifice layer as an effective dirty stop for performing flattening etching. By this It has the process which leaves the pillar of the trench packing material which projects upwards relatively to the top face of a substrate, and the process which etches alternatively the above-mentioned pillar which carries out a protrusion to the top face of the above-mentioned substrate.
[0014] If it says to a detail, according to another description of this invention, furthermore, the approach for forming a substrate separation trench The process which prepares on a substrate the layer which has the thickness as which the 1st was chosen and consists of the 1st ingredient, The process which prepares the layer which has the thickness as which the 2nd was chosen and consists of polish recon above the above-mentioned substrate, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to polish recon on the

layer which consists of the above-mentioned polish recon, The process which etches into a patterning list into the above-mentioned substrate through the above-mentioned sacrifice layer, the layer which consists of the above-mentioned polish recon, and the layer which consists of the 1st ingredient of the above, and forms a separation trench, While making the layer which consists of the oxide which can be etched alternatively to the above-mentioned dirty stop ingredient deposit to the thickness from which the 4th was chosen above the above-mentioned substrate The process which is made to deposit into the above-mentioned separation trench, and is filled up with this separation trench, The process which carries out flattening etching of the above-mentioned trench packing material, using the above-mentioned sacrifice layer as an effective dirty stop for performing flattening etching, The above-mentioned sacrifice layer is alternatively etched from the above-mentioned substrate to the layer which consists of the above-mentioned trench restoration oxide and the above-mentioned polish recon. By this The process which leaves the pillar of the oxide which projects upwards relatively to the layer which consists of polish recon, It has the process which etches alternatively the above-mentioned pillar which carries out a protrusion to the layer which consists of the above-mentioned polish recon, and the process which etches the layer which consists of the above-mentioned polish recon alternatively to the 1st ingredient of the above, and the above-mentioned trench restoration oxide from the above-mentioned substrate.

[0015] According to still more nearly another description of this invention, the approach for forming a substrate separation trench The process which prepares on a substrate the 1st layer which has the thickness as which the 1st was chosen and consists of an oxide, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to oxide on the above-mentioned oxide layer which consists of polish recon, The process which etches into a patterning list into the above-mentioned substrate through the layer which consists of the above-mentioned sacrifice layer and the above-mentioned oxide, and forms a separation trench, While making the layer which consists of the polish recon which can be etched alternatively to the process which prepares the insulating layer which coats a trench into the above-mentioned trench, and the above-mentioned dirty stop ingredient deposit to the thickness from which the 4th was chosen above the above-mentioned substrate The process which is made to deposit into the above-mentioned separation trench, and is filled up with this separation trench, The process which carries out flattening etching of the above-mentioned trench restoration polish recon, using the above-mentioned sacrifice layer as an effective dirty stop for performing flattening etching, The above-mentioned sacrifice layer is alternatively etched from the above-mentioned substrate to the 1st layer which consists of the above-mentioned trench restoration polish recon and the above-mentioned oxide. By this It has the process which leaves the pillar of the polish recon which projects upwards relatively to the 1st layer of the above which consists of an oxide, and the process which etches alternatively the above-mentioned pillar which carries out a protrusion to the 1st layer which consists of the above-mentioned oxide.

[0016]

[Example] With reference to a drawing, the desirable example of this invention is explained below.

[0017] If it explains to a detail more with reference to drawing 6 thru/or drawing 13 , the whole semi-conductor substrate in down stream processing with this invention is shown by the reference mark 30, and a part of this semi-conductor substrate consists of big substrate ingredients 32, i.e., a bulk substrate. As for the bulk substrate 32, generally, it is desirable to consist of silicon (that is, for dopant concentration 2x1015 atom / cm3) which received slight conductive doping processing. The 1st ingredient layer 34 is formed in the crowning of the bulk substrate 32 so that it may have the thickness as which the 1st was chosen. As for the layer 34 of this example, it is desirable to consist of oxides of the SiO2 grade vapor-deposited [were vapor-deposited and it heat-grew up]. As for the thickness as which the above 1st was chosen, it is desirable that it is about 500A from about 100A.

[0018] The 2nd ingredient layer 36 is formed on a layer 34 in the upper part of a substrate so that it may have the thickness as which the 2nd was chosen. The 2nd ingredient layer 36 can be

alternatively etched to the 1st ingredient layer 34. As an example, a desirable ingredient is polish recon, and, as for the thickness as which the above 2nd was chosen, it is desirable that it is about 1000A from about 100A. In the following publications, it explains as that to which a layer 36 forms the top face 37 of a substrate.

[0019] The sacrifice layer 38 which consists of the selected dirty stop (etching halt) ingredient is formed on the 2nd ingredient layer 36 in the upper part of a substrate so that it may have the thickness as which the 3rd was chosen. As for a dirty stop ingredient, it is desirable to be able to etch alternatively to the 2nd ingredient and to consist of nitrides like Si3N4. As for the thickness as which the above 3rd was chosen, it is desirable that it is about 3000A from about 500A.

[0020] If drawing 7 is referred to, patterning is carried out, and sequential etching will be carried out and the sacrifice layer 38, the 2nd ingredient layer 36, the 1st ingredient layer 34, and the bulk substrate 32 will form the separation trench 40. If required, the implant 26 of the conventional technique shown in drawing 3 and the same separation implant can be prepared in the base of a trench 40.

[0021] It is filled up with the interior of the separation trench 40, while the trench packing material layer 42 will deposit above a substrate so that it may have the thickness as which the 4th was chosen if drawing 8 is referred to. A trench packing material can be alternatively etched to the 2nd ingredient, and can also etch the 2nd ingredient alternatively to a trench packing material. Moreover, a dirty stop ingredient can be alternatively etched to a trench packing material. The example of the desirable trench packing material in this example is an oxide like SiO2. Such an oxide can be made to deposit with the technique of the common knowledge like TEOS vacuum evaporationo, and can be doped in boron and/or Lynn if needed. As for the thickness as which the above 4th was chosen, it is desirable that it is about 3000A from about 2000A according to the dimension of a trench. For example, if a trench becomes shallow, the thickness as which the desirable 4th was chosen will also become thin.

[0022] If drawing 9 is referred to, the sacrifice layer 38 is used as an effective dirty stop for flattening etching, and the flattening etching technique is given to the layer 42. The very desirable flattening etching technique in this invention is polish (CMP) like chemical machinery. The example of a CMP slurry in case a layer 42 consists of oxides and a layer 38 consists of nitrides is a slurry which contains SiO2 of abrasiveness in KOH. Such a slurry brings about the etch rate of 0.3 microns per for 1 minute, and forms the structure shown in drawing 9 .

[0023] If drawing 10 is referred to, the sacrifice layer 38 is relatively etched from a substrate alternatively to the 2nd ingredient layer 36 and trench packing material 42, and the pillar 44 of the trench packing material which projects in the upper part from the 2nd ingredient layer 36 is left behind. Thus, the sacrifice layer 38 is etched from a substrate and the pillar of the trench packing material which projects upwards relatively to the top face of the substrate like a front face 37 is formed.

[0024] If drawing 11 is referred to, the projecting pillar 44 was relatively etched alternatively to the top face 37 of a substrate corresponding to this to the 2nd ingredient layer 36, and the ingredient 42 remains into the trench 40. As for such etching, like illustration, it is desirable to perform by etching a pillar 44 to the upper height higher than the top face of the silicon substrate ingredient 32 namely, whose 2nd ingredient layer 36 is a lower part immediately.

[0025] Reference of drawing 12 etches the 2nd ingredient layer 36 from the substrate alternatively relatively to the 1st ingredient layer 34 and trench packing material. The example of etching conditions in case a layer 36 consists of polish recons is using the chemical action of wet polish recon HF / HNO3/H2O which shows the selectivity which was excellent to the oxide.

[0026] If drawing 13 is referred to, dealing with a layer 34 and this etc. is by carrying out, the trench ingredient 42 of thickness is etched, and a separation trench 40 like illustration is brought about.

[0027] The alternative-process of this invention is shown in drawing 14 thru/or drawing 1919 . In the proper range, drawing 6 thru/or the same reference mark as the reference mark of the layer of the example of drawing 13 are used. Drawing 1414 shows alternative substrate 30a in which the trench 40 is formed. The point that the example of drawing 14 differs from the 1st example shown in drawing 7 is that the polish recon layer like the layer 36 of drawing 7 is not prepared at

all. Other layers are as being shown in the example of drawing 6 thru/or drawing 13 . If required, the implant of the conventional technique shown in drawing 3 and the same separation implant can be prepared in the base of a trench 40.
[0028] Reference of drawing 15 forms the trench coating 50 made from an insulating material in the side attachment wall of a trench, and the perimeter of a base at the inside list of the side attachment wall of a trench 40. It is made to grow up by making oxidation conditions expose substrate 30a, i.e., the trench coating 50 can be formed.
[0029] If drawing 16 is referred to, layer 42a of a trench packing material with desirable being formed from polish recon has accumulated to the thickness as which the 4th was chosen. Since layer 42a consists of polish recons formed from the same main ingredients as the bulk substrate 32 of silicon in this example, the trench coating 50 of the ingredient insulated namely, separated was formed, and the bulk substrate 32 (silicon) has prevented contacting polish recon ingredient 42a in a trench 40.
[0030] When drawing 17 is referred to, layer 42a has received flattening etching and it is desirable that CMP performs this etching, using the dirty stop layer 38 as an effective dirty stop to such flattening etching.
[0031] If drawing 18 is referred to, to trench restoration polish recon and the 1st oxide layer 34, relatively, the sacrifice layer 38 was alternatively etched from the substrate, and has left the projected pillar 44 which consists of ingredient 42a.
[0032] Reference of drawing 19 etches the projecting pillar 44 alternatively relatively to the 1st oxide layer 34. It is necessary to notice this alternative example about eliminating the need of making the additional layer 36 depositing, and bringing about the trench coating layer 50. The thickness of ingredient 42a equal to a layer 34 and this after that can be etched from a wafer if needed.
[0033] An above-mentioned technique brings about the effectiveness superior to the conventional technique, and offers the comparatively flat trench packing material which is in the same flat surface as the edge of the front face/trench of silicon especially. a trench -- it is un-obvious and the reason is that a transistor makes etchback of a trench packing material possible after CMP or other flattening etching after that by use of the above-mentioned dirty stop ingredient, without having a bad influence on that it is new to combine that it is dirty and to use the dirty stop ingredient of this invention, and the silicon front face in which it is formed.
[0034]
[Effect of the Invention] According to this invention, the outstanding substrate separation trench can be formed.

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1] The process which has the selected thickness and prepares on a substrate the layer which consists of the selected ingredient in the semi-conductor art for forming a substrate separation trench, The process which prepares the sacrifice layer which has the selected thickness and consists of the selected dirty stop ingredient on the layer which consists of said selected ingredient, The process which etches into a patterning list into said substrate through the layer which consists of said sacrifice layer and said selected ingredient, and forms a separation trench, The process which the upper part list of said substrate is made to deposit the trench packing material which has the selected thickness into said separation trench, and is filled up with said separation trench, Said sacrifice layer is etched from the process which carries out flattening etching of said trench packing material, and said substrate, using said sacrifice layer as an effective dirty stop for performing flattening etching. By this The semi-conductor art for forming a substrate separation trench equipped with the process which leaves the pillar of the trench packing material which projects upwards relatively to the top face of a substrate, and the process which etches said projecting pillar alternatively to the top face of said substrate.
[Claim 2] The semi-conductor art for forming the substrate separation trench characterized by said process which carries out flattening etching including the polish processing like chemical machinery in the semi-conductor art for forming the substrate separation trench of claim 1.
[Claim 3] The semi-conductor art for forming the substrate separation trench characterized by said selected ingredient containing polish recon in the semi-conductor art for forming the substrate separation trench of claim 1.
[Claim 4] A semi-conductor art for said selected thickness of said selected ingredient to form [said selected ingredient] the substrate separation trench characterized by being about 500A from about 100A including an oxide in the semi-conductor art for forming the substrate separation trench of claim 1.
[Claim 5] The process which prepares on a substrate the layer which has the thickness as which the 1st was chosen in the semi-conductor art for forming a substrate separation trench, and consists of the 1st ingredient, The process which prepares the layer which has the thickness as which the 2nd was chosen and consists of the 2nd ingredient which can be etched alternatively to said 1st ingredient above said substrate, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to said 2nd ingredient on the layer which consists of said 2nd ingredient, The process which etches into a patterning list into said substrate through said sacrifice layer, the layer which consists of said 2nd ingredient, and the layer which consists of said 1st ingredient, and forms a separation trench, It is the trench packing material which can be etched alternatively to said 2nd ingredient. Said 2nd ingredient can be alternatively etched to this trench packing material. Moreover, while said dirty stop ingredient makes the layer which consists of the trench packing material which can be etched alternatively to this trench packing material deposit to the thickness from which the 4th was chosen above said substrate The process made to deposit into said separation trench, and the process which carries out flattening etching of said trench packing material, using said sacrifice layer as an effective dirty

stop for performing flattening etching, Said sacrifice layer is alternatively etched from said substrate to said the 2nd ingredient and said trench packing material. By this The process which leaves the pillar of the trench packing material which projects upwards relatively to the layer which consists of said 2nd ingredient of a substrate, The semi-conductor art for forming a substrate separation trench equipped with the process which etches said projecting pillar alternatively to the layer which consists of said 2nd ingredient, and the process which etches said 2nd ingredient from said substrate alternatively to said the 1st ingredient and said trench packing material.

[Claim 6] The semi-conductor art for forming the substrate separation trench characterized by said 1st ingredient containing oxide in the semi-conductor art for forming the substrate separation trench of claim 5.

[Claim 7] The semi-conductor art for forming the substrate separation trench characterized by said 2nd ingredient containing polish recon in the semi-conductor art for forming the substrate separation trench of claim 5.

[Claim 8] A semi-conductor art for the process which etches said projecting pillar to form the substrate separation trench characterized by including the phase which etches said pillar caudad to the height of the lower part of the layer which consists of said 2nd ingredient in the semi-conductor art for forming the substrate separation trench of claim 5.

[Claim 9] The process which prepares on a substrate the layer which has the thickness as which the 1st was chosen in the semi-conductor art for forming a substrate separation trench, and consists of the 1st ingredient, The process which prepares the layer which has the thickness as which the 2nd was chosen and consists of polish recon above said substrate, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to polish recon on the layer which consists of said polish recon, The process which etches into a patterning list into said substrate through said sacrifice layer, the layer which consists of said polish recon, and the layer which consists of said 1st ingredient, and forms a separation trench, While making the layer which consists of the oxide which can be etched alternatively to said dirty stop ingredient deposit to the thickness from which the 4th was chosen above said substrate The process which is made to deposit into said separation trench and is filled up with this separation trench, The process which carries out flattening etching of said trench packing material, using said sacrifice layer as an effective dirty stop for performing flattening etching, Said sacrifice layer is alternatively etched from said substrate to the layer which consists of said trench restoration oxide and said polish recon. By this The process which leaves the pillar of the oxide which projects upwards relatively to the layer which consists of polish recon, The process which etches said projecting pillar alternatively to the layer which consists of said polish recon, The semi-conductor art for forming a substrate separation trench equipped with the process which etches the layer which consists of said polish recon alternatively to said the 1st ingredient and said trench restoration oxide from said substrate.

[Claim 10] A semi-conductor art for the process which etches said projecting pillar to form the substrate separation trench characterized by including the phase which etches said pillar caudad to the height of the lower part of the layer which consists of said polish recon in the semi-conductor art for forming the substrate separation trench of claim 9.

[Claim 11] The process which prepares on a substrate the 1st layer which has the thickness as which the 1st was chosen in the semi-conductor art for forming a substrate separation trench, and consists of an oxide, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to oxide on said oxide layer which consists of polish recon, The process which etches into a patterning list into said substrate through the layer which consists of said sacrifice layer and said oxide, and forms a separation trench, While making the layer which consists of the polish recon which can be etched alternatively to the process which prepares the insulating layer which coats a trench into said trench, and said dirty stop ingredient deposit to the thickness from which the 4th was chosen above said substrate The process which is made to deposit into said separation trench and is filled up with this separation trench, The process

which carries out flattening etching of said trench restoration polish recon, using said sacrifice layer as an effective dirty stop for performing flattening etching, Said sacrifice layer is alternatively etched from said substrate to the 1st layer which consists of said trench restoration polish recon and said oxide. By this The semi-conductor art for forming a substrate separation trench equipped with the process which leaves the pillar of the polish recon which projects upwards relatively to said 1st layer which consists of an oxide, and the process which etches said projecting pillar alternatively to the 1st layer which consists of said oxide.

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CLAIMS

[Claim(s)]
[Claim 1] The process which has the selected thickness and prepares on a substrate the layer which consists of the selected ingredient in the semi-conductor art for forming a substrate separation trench, The process which prepares the sacrifice layer which has the selected thickness and consists of the selected dirty stop ingredient on the layer which consists of said selected ingredient, The process which etches into a patterning list into said substrate through the layer which consists of said sacrifice layer and said selected ingredient, and forms a separation trench, The process which the upper part list of said substrate is made to deposit the trench packing material which has the selected thickness into said separation trench, and is filled up with said separation trench, Said sacrifice layer is etched from the process which carries out flattening etching of said trench packing material, and said substrate, using said sacrifice layer as an effective dirty stop for performing flattening etching. By this The semi-conductor art for forming a substrate separation trench equipped with the process which leaves the pillar of the trench packing material which projects upwards relatively to the top face of a substrate, and the process which etches said projecting pillar alternatively to the top face of said substrate.
[Claim 2] The semi-conductor art for forming the substrate separation trench characterized by said process which carries out flattening etching including the polish processing like chemical machinery in the semi-conductor art for forming the substrate separation trench of claim 1.
[Claim 3] The semi-conductor art for forming the substrate separation trench characterized by said selected ingredient containing polish recon in the semi-conductor art for forming the substrate separation trench of claim 1.
[Claim 4] A semi-conductor art for said selected thickness of said selected ingredient to form [said selected ingredient] the substrate separation trench characterized by being about 500A from about 100A including an oxide in the semi-conductor art for forming the substrate separation trench of claim 1.
[Claim 5] The process which prepares on a substrate the layer which has the thickness as which the 1st was chosen in the semi-conductor art for forming a substrate separation trench, and consists of the 1st ingredient, The process which prepares the layer which has the thickness as which the 2nd was chosen and consists of the 2nd ingredient which can be etched alternatively to said 1st ingredient above said substrate, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to said 2nd ingredient on the layer which consists of said 2nd ingredient, The process which etches into a patterning list into said substrate through said sacrifice layer, the layer which consists of said 2nd ingredient, and the layer which consists of said 1st ingredient, and forms a separation trench, It is the trench packing material which can be etched alternatively to said 2nd ingredient. Said 2nd ingredient can be alternatively etched to this trench packing material. Moreover, while said dirty stop ingredient makes the layer which consists of the trench packing material which can be etched alternatively to this trench packing material deposit to the thickness from which the 4th was chosen above said substrate The process made to deposit into said separation trench, and the process which carries out flattening etching of said trench packing material, using said sacrifice layer as an effective dirty

stop for performing flattening etching, Said sacrifice layer is alternatively etched from said substrate to said the 2nd ingredient and said trench packing material. By this The process which leaves the pillar of the trench packing material which projects upwards relatively to the layer which consists of said 2nd ingredient of a substrate, The semi-conductor art for forming a substrate separation trench equipped with the process which etches said projecting pillar alternatively to the layer which consists of said 2nd ingredient, and the process which etches said 2nd ingredient from said substrate alternatively to said the 1st ingredient and said trench packing material.

[Claim 6] The semi-conductor art for forming the substrate separation trench characterized by said 1st ingredient containing oxide in the semi-conductor art for forming the substrate separation trench of claim 5.

[Claim 7] The semi-conductor art for forming the substrate separation trench characterized by said 2nd ingredient containing polish recon in the semi-conductor art for forming the substrate separation trench of claim 5.

[Claim 8] A semi-conductor art for the process which etches said projecting pillar to form the substrate separation trench characterized by including the phase which etches said pillar caudad to the height of the lower part of the layer which consists of said 2nd ingredient in the semi-conductor art for forming the substrate separation trench of claim 5.

[Claim 9] The process which prepares on a substrate the layer which has the thickness as which the 1st was chosen in the semi-conductor art for forming a substrate separation trench, and consists of the 1st ingredient, The process which prepares the layer which has the thickness as which the 2nd was chosen and consists of polish recon above said substrate, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to polish recon on the layer which consists of said polish recon, The process which etches into a patterning list into said substrate through said sacrifice layer, the layer which consists of said polish recon, and the layer which consists of said 1st ingredient, and forms a separation trench, While making the layer which consists of the oxide which can be etched alternatively to said dirty stop ingredient deposit to the thickness from which the 4th was chosen above said substrate The process which is made to deposit into said separation trench and is filled up with this separation trench, The process which carries out flattening etching of said trench packing material, using said sacrifice layer as an effective dirty stop for performing flattening etching, Said sacrifice layer is alternatively etched from said substrate to the layer which consists of said trench restoration oxide and said polish recon. By this The process which leaves the pillar of the oxide which projects upwards relatively to the layer which consists of polish recon, The process which etches said projecting pillar alternatively to the layer which consists of said polish recon, The semi-conductor art for forming a substrate separation trench equipped with the process which etches the layer which consists of said polish recon alternatively to said the 1st ingredient and said trench restoration oxide from said substrate.

[Claim 10] A semi-conductor art for the process which etches said projecting pillar to form the substrate separation trench characterized by including the phase which etches said pillar caudad to the height of the lower part of the layer which consists of said polish recon in the semi-conductor art for forming the substrate separation trench of claim 9.

[Claim 11] The process which prepares on a substrate the 1st layer which has the thickness as which the 1st was chosen in the semi-conductor art for forming a substrate separation trench, and consists of an oxide, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to oxide on said oxide layer which consists of polish recon, The process which etches into a patterning list into said substrate through the layer which consists of said sacrifice layer and said oxide, and forms a separation trench, While making the layer which consists of the polish recon which can be etched alternatively to the process which prepares the insulating layer which coats a trench into said trench, and said dirty stop ingredient deposit to the thickness from which the 4th was chosen above said substrate The process which is made to deposit into said separation trench and is filled up with this separation trench, The process

which carries out flattening etching of said trench restoration polish recon, using said sacrifice layer as an effective dirty stop for performing flattening etching, Said sacrifice layer is alternatively etched from said substrate to the 1st layer which consists of said trench restoration polish recon and said oxide. By this The semi-conductor art for forming a substrate separation trench equipped with the process which leaves the pillar of the polish recon which projects upwards relatively to said 1st layer which consists of an oxide, and the process which etches said projecting pillar alternatively to the 1st layer which consists of said oxide.

[Translation done.]

PRIOR ART

[Description of the Prior Art] An integrated circuit is accumulated chemically and physically by substrates, such as a silicon wafer, by carrying out patterning of the field of a substrate, and carrying out patterning of the layer on a substrate. The above-mentioned field and a layer can be made into conductivity, and a conductor and resistance can be manufactured. Moreover, the conductivity of a type which is different in the above-mentioned field and a layer can be given, and this is a transistor and requirements indispensable to manufacture of diode. When forming into a substrate, various circuit elements, i.e., device, it is necessary to separate namely, insulate such a device of each other.

[0003] In case an integrated circuit is manufactured, the various techniques for insulating electrically the device formed into the bulk substrate have been developed. The technique of a certain developed common knowledge omits partial oxidation (LOcal Oxidation of Silicon) of silicon, is called LOCOS separation, and forms the oxide of a half-hollow mold in the non active (or field) field of a substrate in this technique. The principle of the LOCOS method is growing up an oxide into a desired field field alternatively. Growth of such oxide is performed by covering an active field by the film of silicon nitride, and the film of the above-mentioned silicon nitride prevents that oxidation takes place under it. The layer of a nitride exposes up patterning and the silicon field by which it is etched and a field oxide is needed in it, and is grown up. Then, a wafer is exposed on oxidation conditions. An oxidant grows up to be a part without a masking nitride. However, in the periphery section of masking of a nitride, that oxide is spread a little in the side.

[0004] Thereby, an oxide grows under the periphery section of a nitride and this periphery section is raised. The configuration of the oxide of the periphery section of a nitride forms the wedge of the oxide which inclines gently, and this wedge joins the oxide layer of a lower layer pad. The above-mentioned wedge is called the beak (bird's beak) of a bird. It elongates to the side of field oxide and the beak of a bird goes into the active field of a device. One of such the faults of separation technology is producing the field oxide which has the dimension of the longitudinal direction where the beak of the above-mentioned bird is bigger than the lower limit of the photograph function it being used in order to form mask opening in a nitride.

[0005] Therefore, it takes for the geometric configuration of a device to approach a submicron dimension, and the effectiveness of the usual LOCOS separation technology approaches the limitation, and CMOS and the alternative separation process for bipolar techniques are needed. There is trench separation as one of such the techniques. In this technique, it fills up, and the separated trench is perpendicularly arranged in a substrate, and separates namely, insulates the electric device in the both sides of this trench. This invention relates to the art for forming the substrate separation trench like ****.

[0006] The trouble accompanying the technique is explained to a separation trench technical list with the conventional technique with reference to drawing 1 thru/or drawing 5 . Drawing 1 shows the semi-conductor substrate 10 which consists of a bulk substrate 12, a film 14 of pad oxide, and a layer 16 of a photoresist. Patterning of the photoresist layer 16 will be carried out, it will form the contact opening 20, and the trench which penetrates this will be formed in this opening.

[0007] If drawing 2 is referred to, the pad oxide layer 14 and the bulk substrate 12 will be etched

like illustration, and will form dead air space 22, i.e., a trench.
[0008] Reference of drawing 3 is growing up the layer 24 of SiO2 in a trench 22.
[0009] Like illustration, the additional separation implant 26 can also be formed in the base of a trench 22. For example, when the bulk substrate 12 consists of silicon with which the device of n channels will be formed (p-), the implant 26 can be made into the implant (p+) and the electric separation effectiveness, i.e., the insulating effectiveness, can be further brought about between the circuit elements which should be formed in the both sides of a trench 22. Before the implant generally removes the mask layer shown in drawing 1 , it is prepared.
[0010] If drawing 4 is referred to, the layer 28 which consists of a trench packing material would be formed in the crowning of a wafer, and will be filled up with the trench 22. The ingredient of a layer 28 can be used as the polish recon which has ** filled up with the volume of a trench 22, an oxide, or other ingredients. It is not necessary to necessarily make the ingredient of a layer 28 into an insulating material. The reason is that the layer 26 of oxide brings the electric insulating effectiveness to the field of the side of a trench 22. Generally such a layer is deposited in the shape of conformal, and forms the part 30 of a hollow like illustration, i.e., a V character mold.
[0011] If drawing 5 is referred to, a layer 28 will be exposed by proper etching and will be removed to the point of leaving the trench 22 with which it filled up in general. However, generally partial 30a of a V character mold remains like illustration also after etching with the property deposited in the shape of [of a layer 28] conformal, and this is not desirable.

[Translation done.]

* NOTICES *

TECHNICAL FIELD

[Industrial Application] This invention relates to the trench separation approach in semi-conductor processing.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, the outstanding substrate separation trench can be formed.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] It is desirable to improve the above-mentioned technique and other above-mentioned techniques which form a substrate separation trench.
[0013]

[Translation done.]

* NOTICES *

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MEANS

[Means for Solving the Problem] According to the description with this invention, the semi-conductor art for forming a substrate separation trench The process which prepares on a substrate the layer which has the selected thickness and consists of the selected ingredient, The process which prepares the sacrifice layer which has the selected thickness and consists of the selected dirty stop ingredient on the layer which consists of the ingredient by which selection was made [above-mentioned], The process which etches into a patterning list into the above-mentioned substrate through the layer which consists of the above-mentioned sacrifice layer and the ingredient by which selection was made [above-mentioned], and forms a separation trench, The process which the upper part list of the above-mentioned substrate is made to deposit the trench packing material which has the selected thickness into the above-mentioned separation trench, and is filled up with the above-mentioned separation trench, The above-mentioned sacrifice layer is etched from the process which carries out flattening etching of the above-mentioned trench packing material, and the above-mentioned substrate, using the above-mentioned sacrifice layer as an effective dirty stop for performing flattening etching. By this It has the process which leaves the pillar of the trench packing material which projects upwards relatively to the top face of a substrate, and the process which etches alternatively the above-mentioned pillar which carries out a protrusion to the top face of the above-mentioned substrate.
[0014] If it says to a detail, according to another description of this invention, furthermore, the approach for forming a substrate separation trench The process which prepares on a substrate the layer which has the thickness as which the 1st was chosen and consists of the 1st ingredient, The process which prepares the layer which has the thickness as which the 2nd was chosen and consists of polish recon above the above-mentioned substrate, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to polish recon on the layer which consists of the above-mentioned polish recon, The process which etches into a patterning list into the above-mentioned substrate through the above-mentioned sacrifice layer, the layer which consists of the above-mentioned polish recon, and the layer which consists of the 1st ingredient of the above, and forms a separation trench, While making the layer which consists of the oxide which can be etched alternatively to the above-mentioned dirty stop ingredient deposit to the thickness from which the 4th was chosen above the above-mentioned substrate The process which is made to deposit into the above-mentioned separation trench, and is filled up with this separation trench, The process which carries out flattening etching of the above-mentioned trench packing material, using the above-mentioned sacrifice layer as an effective dirty stop for performing flattening etching, The above-mentioned sacrifice layer is alternatively etched from the above-mentioned substrate to the layer which consists of the above-mentioned trench restoration oxide and the above-mentioned polish recon. By this The process which leaves the pillar of the oxide which projects upwards relatively to the layer which consists of polish recon, It has the process which etches alternatively the above-mentioned pillar which carries out a protrusion to the layer which consists of the above-mentioned polish recon, and the process which etches the layer which consists of the above-mentioned polish

recon alternatively to the 1st ingredient of the above, and the above-mentioned trench restoration oxide from the above-mentioned substrate.
[0015] According to still more nearly another description of this invention, the approach for forming a substrate separation trench The process which prepares on a substrate the 1st layer which has the thickness as which the 1st was chosen and consists of an oxide, The process which prepares the sacrifice layer which has the thickness as which the 3rd was chosen and consists of the selected dirty stop ingredient which can be etched alternatively to oxide on the above-mentioned oxide layer which consists of polish recon, The process which etches into a patterning list into the above-mentioned substrate through the layer which consists of the above-mentioned sacrifice layer and the above-mentioned oxide, and forms a separation trench, While making the layer which consists of the polish recon which can be etched alternatively to the process which prepares the insulating layer which coats a trench into the above-mentioned trench, and the above-mentioned dirty stop ingredient deposit to the thickness from which the 4th was chosen above the above-mentioned substrate The process which is made to deposit into the above-mentioned separation trench, and is filled up with this separation trench, The process which carries out flattening etching of the above-mentioned trench restoration polish recon, using the above-mentioned sacrifice layer as an effective dirty stop for performing flattening etching, The above-mentioned sacrifice layer is alternatively etched from the above-mentioned substrate to the 1st layer which consists of the above-mentioned trench restoration polish recon and the above-mentioned oxide. By this It has the process which leaves the pillar of the polish recon which projects upwards relatively to the 1st layer of the above which consists of an oxide, and the process which etches alternatively the above-mentioned pillar which carries out a protrusion to the 1st layer which consists of the above-mentioned oxide.

[Translation done.]

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DESCRIPTION OF DRAWINGS

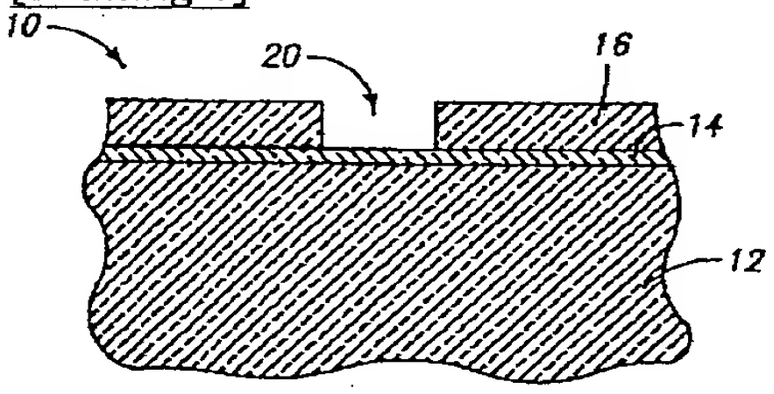
[Brief Description of the Drawings]
[Drawing 1] It is the rough sectional view of the fragment of the semiconductor wafer processed according to the approach of the conventional technique explained by the term of a Prior art.
[Drawing 2] It is the sectional view showing the wafer of drawing 1 in down stream processing of the next conventional technique of down stream processing shown in drawing 1 .
[Drawing 3] It is the sectional view showing the wafer of drawing 1 in down stream processing of the next conventional technique of down stream processing shown in drawing 2 .
[Drawing 4] It is the sectional view showing the wafer of drawing 1 in down stream processing of the next conventional technique of down stream processing shown in drawing 3 .
[Drawing 5] It is the sectional view showing the wafer of drawing 1 in down stream processing of the next conventional technique of down stream processing shown in drawing 4 .
[Drawing 6] It is the rough sectional view showing the fragment of the semiconductor wafer in down stream processing with this invention.
[Drawing 7] It is the sectional view showing the wafer of drawing 6 in the next down stream processing of down stream processing shown in drawing 6 .
[Drawing 8] It is the sectional view showing the wafer of drawing 6 in the next down stream processing of down stream processing shown in drawing 7 .
[Drawing 9] It is the sectional view showing the wafer of drawing 6 in the next down stream processing of down stream processing shown in drawing 8 .
[Drawing 10] It is the sectional view showing the wafer of drawing 6 R> 6 in the next down stream processing of down stream processing shown in drawing 9 .
[Drawing 11] It is the sectional view showing the wafer of drawing 6 in the next down stream processing of down stream processing shown in drawing 10 .
[Drawing 12] It is the sectional view showing the wafer of drawing 6 in the next down stream processing of down stream processing shown in drawing 11 .
[Drawing 13] It is the sectional view showing the wafer of drawing 6 in the next down stream processing of down stream processing shown in drawing 12 .
[Drawing 14] It is the rough sectional view of the fragment of the semiconductor wafer in down stream processing with the alternative-approach of this invention.
[Drawing 15] It is the sectional view showing the wafer of drawing 14 in the next down stream processing of down stream processing shown in drawing 14 .
[Drawing 16] It is the sectional view showing the wafer of drawing 14 in the next down stream processing of down stream processing shown in drawing 15 .
[Drawing 17] It is the sectional view showing the wafer of drawing 14 in the next down stream processing of down stream processing shown in drawing 16 .
[Drawing 18] It is the sectional view showing the wafer of drawing 14 in the next down stream processing of down stream processing shown in drawing 17 .
[Drawing 19] It is the sectional view showing the wafer of drawing 14 in the next down stream processing of down stream processing shown in drawing 18 .
[Description of Notations]
30 Semi-conductor Substrate 32 Bulk Substrate

34 1st Ingredient Layer 36 2nd Ingredient Layer
37 Top Face of Substrate 38 Sacrifice Layer
40 Trench 42 Trench Packing Material
42 Trench Packing Material Layer 44 Pillar
50 Trench Coating

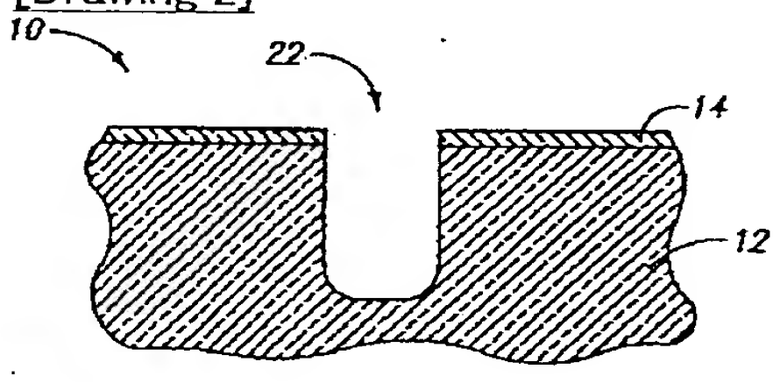
[Translation done.]

DRAWINGS

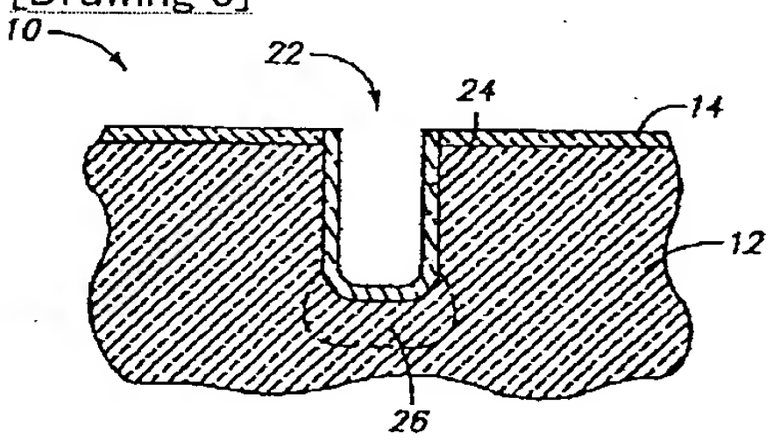
[Drawing 1]



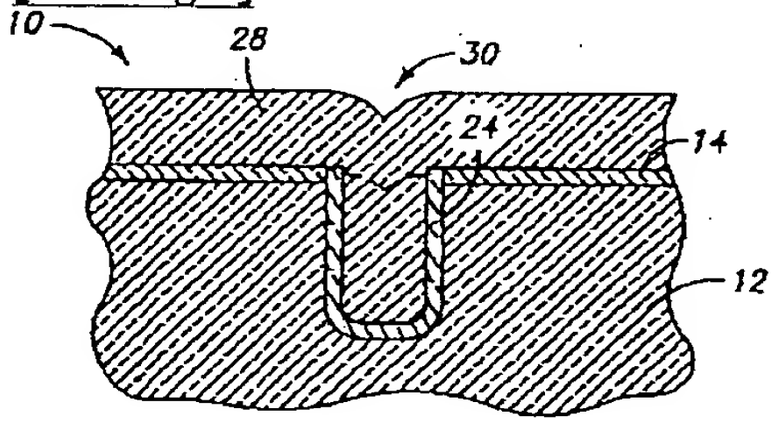
[Drawing 2]



[Drawing 3]



[Drawing 4]



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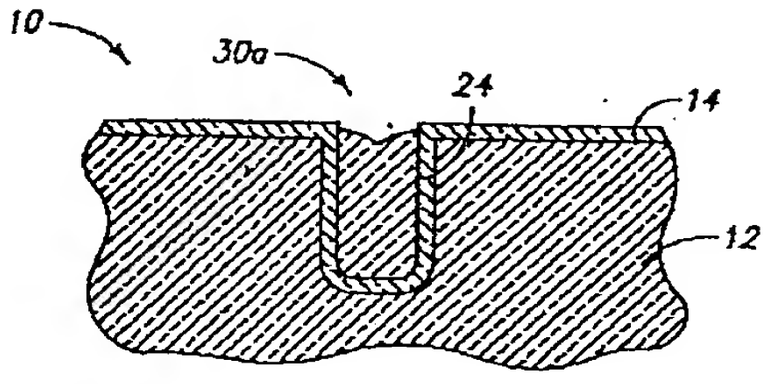

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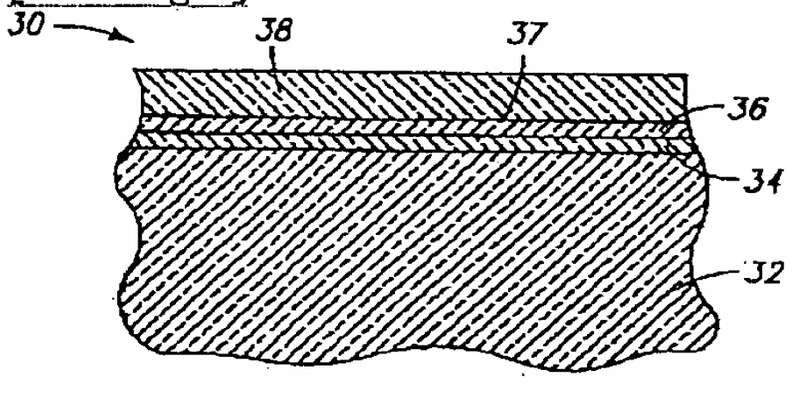

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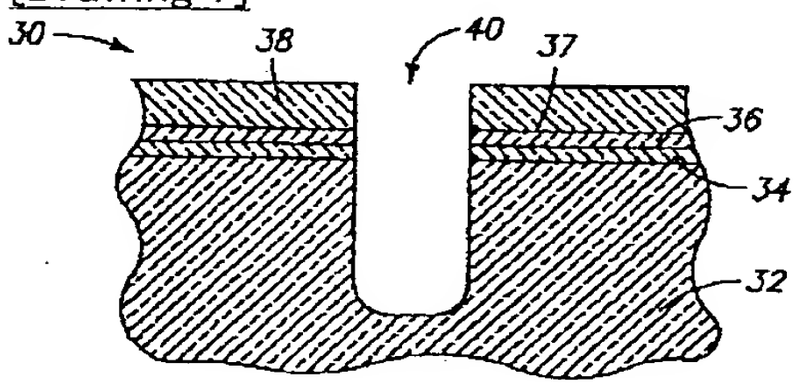

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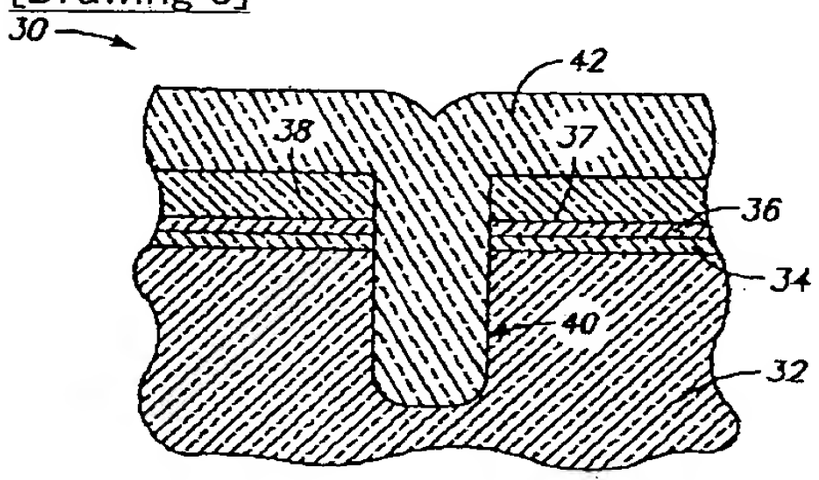

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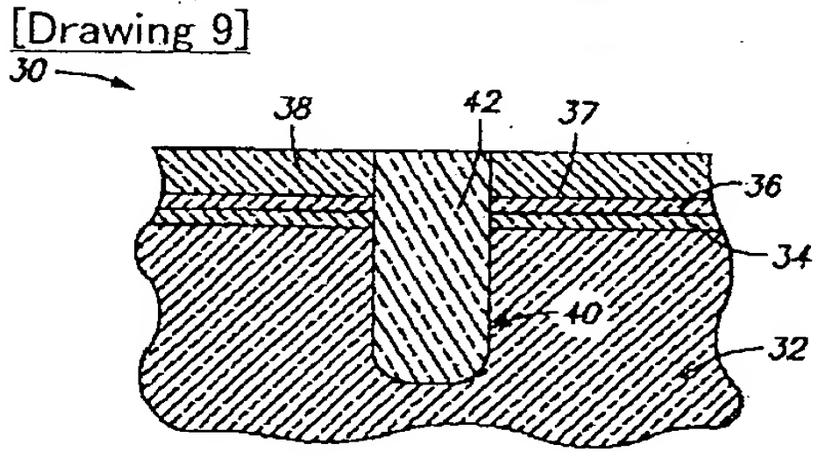
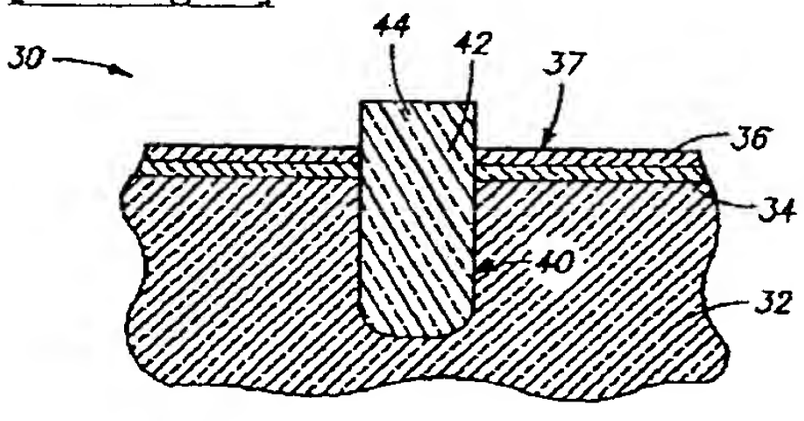


[Drawing 10]



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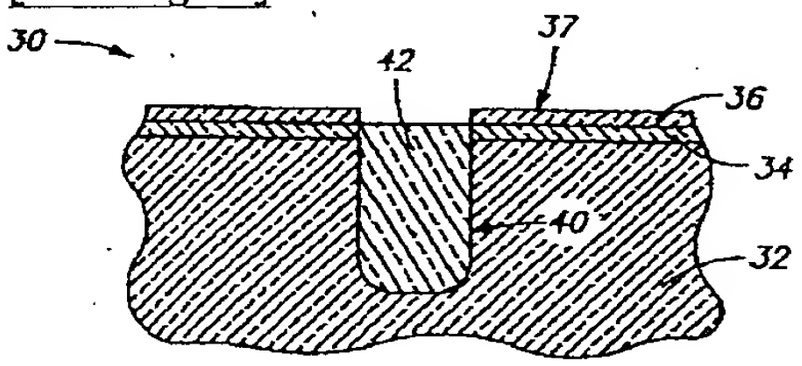

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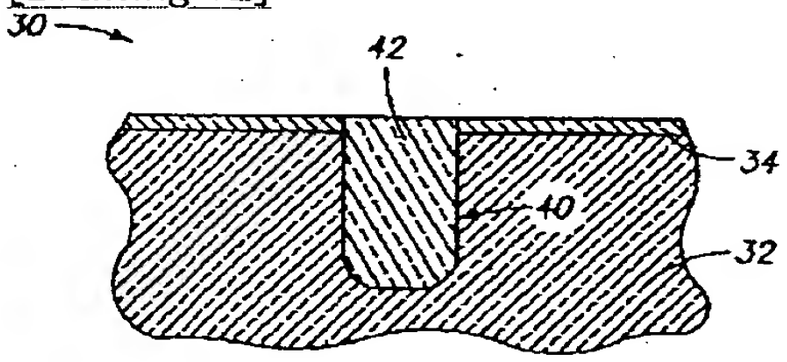
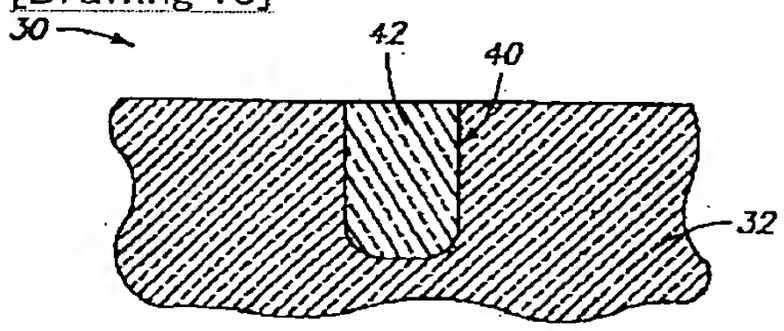


[Drawing 13]



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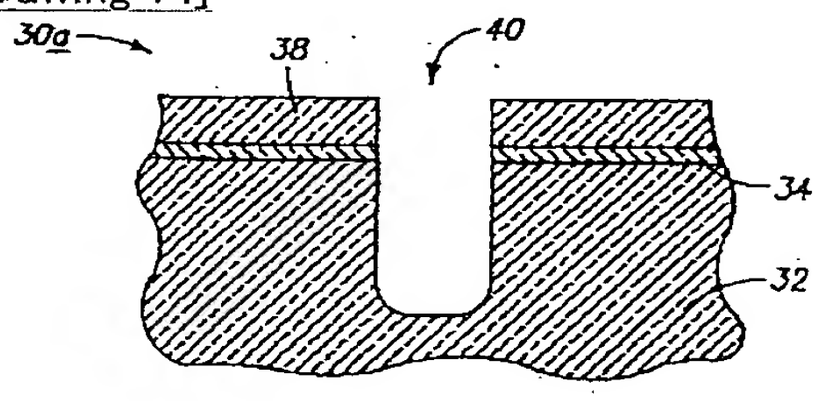

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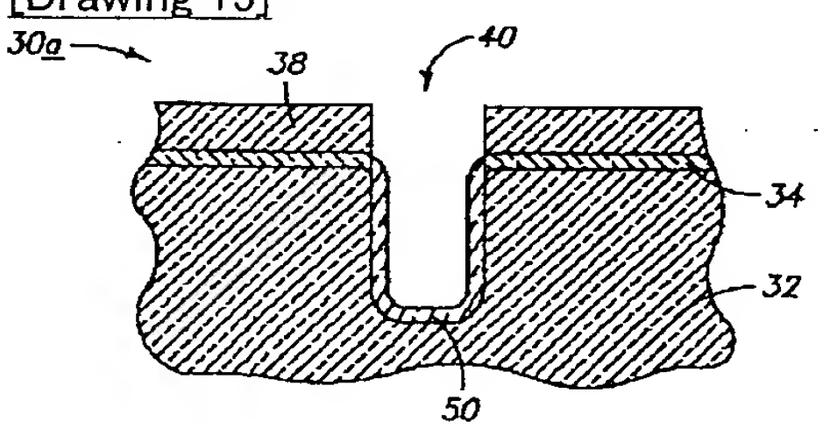

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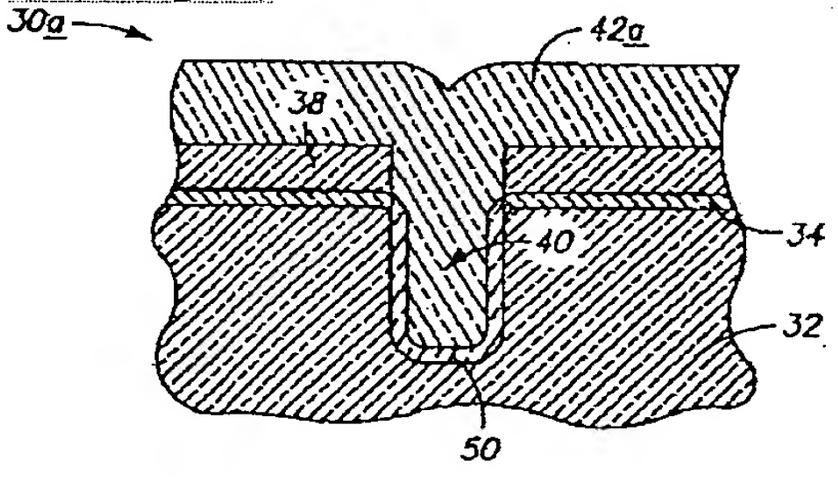
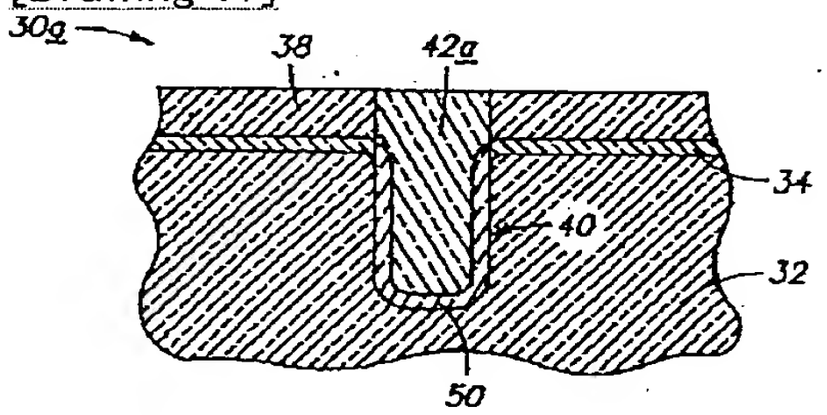
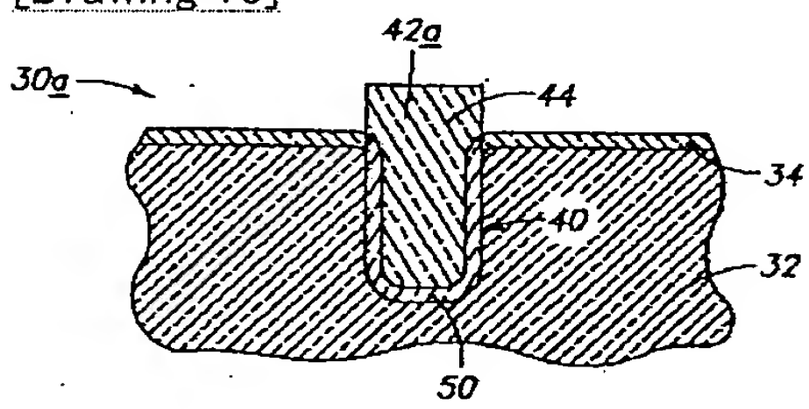


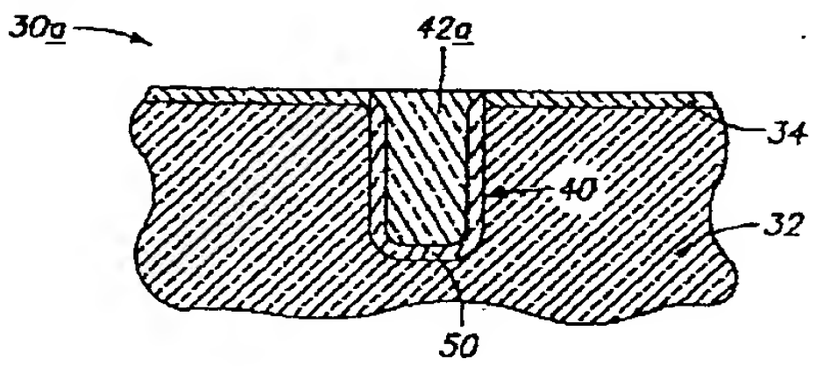
[Drawing 17]



[Drawing 18]



[Drawing 19]



[Translation done.]

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(33)優先権主張国　米国（ＵＳ）

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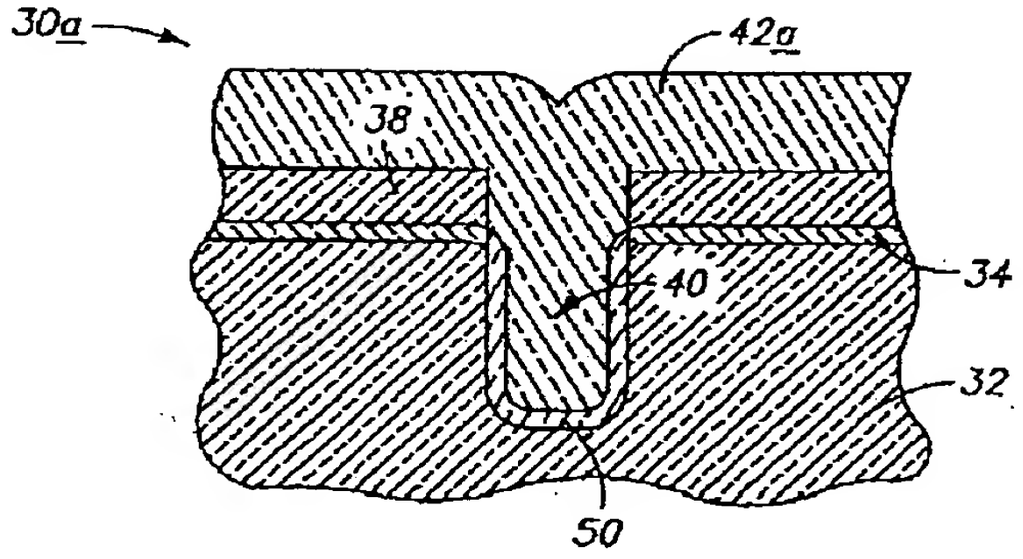
最終頁に続く

(54)【発明の名称】基板分離トレンチを形成するための半導体処理方法

(57)【要約】

【目的】　基板分離トレンチを形成するための半導体処理方法を提供する。

【構成】　本方法は以下の（ａ）－（ｇ）の工程を含む。（ａ）選択された厚みを有する第１の材料層３４を基板３２の上に設ける工程。（ｂ）選択された厚みを有する犠牲層３８を第１の材料層３４の上に設ける工程。（ｃ）犠牲層３８及び第１の材料層３４を通して基板３２の中へパターニング並びにエッチングを行い、分離トレンチ４０を形成する工程。（ｄ）選択された厚みを有するトレンチ充填材料４２ａを基板の上方並びに分離トレンチ４０の中に堆積させ、分離トレンチを充填する工程。（ｅ）エッチストップとして犠牲層３８を用い、トレンチ充填材料４２ａを平坦化エッチングする工程。（ｆ）基板から犠牲層をエッチングし、基板の上面から上方へ突出するピラーを残す工程。（ｇ）ピラーを基板の上面に対して選択的にエッチングする工程。



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【特許請求の範囲】

【請求項１】　基板分離トレンチを形成するための半導体処理方法において、

選択された厚みを有し、選択された材料から成る層を基板の上に設ける工程と、

選択された厚みを有し、選択されたエッチストップ材料から成る犠牲層を前記選択された材料から成る層の上に設ける工程と、

前記犠牲層及び前記選択された材料から成る層を通して前記基板の中へパターニング並びにエッチングを行い、分離トレンチを形成する工程と、

選択された厚みを有するトレンチ充填材料を前記基板の上方並びに前記分離トレンチの中に堆積させ、前記分離トレンチを充填する工程と、

平坦化エッチングを行うための効果的なエッチストップとして前記犠牲層を用い、前記トレンチ充填材料を平坦化エッチングする工程と、

前記基板から前記犠牲層をエッチングし、これにより、基板の上面に対して相対的に上方へ突出するトレンチ充填材料のピラーを残す工程と、

前記突出するピラーを前記基板の上面に対して選択的にエッチングする工程とを備える基板分離トレンチを形成するための半導体処理方法。

【請求項２】　請求項１の基板分離トレンチを形成するための半導体処理方法において、前記平坦化エッチングする工程が、化学機械的な研磨処理を含むことを特徴とする基板分離トレンチを形成するための半導体処理方法。

【請求項３】　請求項１の基板分離トレンチを形成するための半導体処理方法において、前記選択された材料がポリシリコンを含むことを特徴とする基板分離トレンチを形成するための半導体処理方法。

【請求項４】　請求項１の基板分離トレンチを形成するための半導体処理方法において、前記選択された材料が酸化物を含み、前記選択された材料の前記選択された厚みが約１００オングストロームから約５００オングストロームであることを特徴とする基板分離トレンチを形成するための半導体処理方法。

【請求項５】　基板分離トレンチを形成するための半導体処理方法において、

第１の選択された厚みを有し、第１の材料から成る層を基板の上に設ける工程と、

第２の選択された厚みを有し、前記第１の材料に対して選択的にエッチング可能な第２の材料から成る層を前記基板の上方に設ける工程と、

第３の選択された厚みを有し、前記第２の材料に対して選択的にエッチング可能な選択されたエッチストップ材料から成る犠牲層を前記第２の材料から成る層の上に設ける工程と、

前記犠牲層、前記第２の材料から成る層、及び前記第１

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の材料から成る層を通して前記基板の中へパターニング並びにエッチングを行い、分離トレンチを形成する工程と、

前記第２の材料に対して選択的にエッチング可能なトレンチ充填材料であって、前記第２の材料は該トレンチ充填材料に対して選択的にエッチング可能であり、また、前記エッチストップ材料は該トレンチ充填材料に対して選択的にエッチング可能であるトレンチ充填材料から成る層を前記基板の上方に第４の選択された厚みまで堆積させると共に、前記分離トレンチの中に堆積させる工程と、

平坦化エッチングを行うための効果的なエッチストップとして前記犠牲層を用い、前記トレンチ充填材料を平坦化エッチングする工程と、

前記第２の材料及び前記トレンチ充填材料に対して選択的に前記犠牲層を前記基板からエッチングし、これにより、基板の前記第２の材料から成る層に対して相対的に上方へ突出するトレンチ充填材料のピラーを残す工程と、

前記突出するピラーを前記第２の材料から成る層に対して選択的にエッチングする工程と、

前記第１の材料及び前記トレンチ充填材料に対して選択的に前記第２の材料を前記基板からエッチングする工程とを備える基板分離トレンチを形成するための半導体処理方法。

【請求項６】　請求項５の基板分離トレンチを形成するための半導体処理方法において、前記第１の材料が酸化物を含むことを特徴とする基板分離トレンチを形成するための半導体処理方法。

【請求項７】　請求項５の基板分離トレンチを形成するための半導体処理方法において、前記第２の材料がポリシリコンを含むことを特徴とする基板分離トレンチを形成するための半導体処理方法。

【請求項８】　請求項５の基板分離トレンチを形成するための半導体処理方法において、前記突出するピラーをエッチングする工程が、前記第２の材料から成る層の下方の高さまで前記ピラーを下方にエッチングする段階を含むことを特徴とする基板分離トレンチを形成するための半導体処理方法。

【請求項９】　基板分離トレンチを形成するための半導体処理方法において、

第１の選択された厚みを有し、第１の材料から成る層を基板の上に設ける工程と、

第２の選択された厚みを有し、ポリシリコンから成る層を前記基板の上方に設ける工程と、

第３の選択された厚みを有し、ポリシリコンに対して選択的にエッチング可能な選択されたエッチストップ材料から成る犠牲層を前記ポリシリコンから成る層の上に設ける工程と、

前記犠牲層、前記ポリシリコンから成る層、及び前記第

１の材料から成る層を通して前記基板の中へパターニング並びにエッチングを行い、分離トレンチを形成する工程と、
前記エッチストップ材料に対して選択的にエッチング可能な酸化物から成る層を前記基板の上方に第４の選択された厚みまで堆積させると共に、前記分離トレンチの中に堆積させて該分離トレンチを充填する工程と、
平坦化エッチングを行うための効果的なエッチストップとして前記犠牲層を用い、前記トレンチ充填材料を平坦化エッチングする工程と、
前記トレンチ充填酸化物及び前記ポリシリコンから成る層に対して選択的に前記犠牲層を前記基板からエッチングし、これにより、ポリシリコンから成る層に対して相対的に上方へ突出する酸化物のピラーを残す工程と、
前記突出するピラーを前記ポリシリコンから成る層に対して選択的にエッチングする工程と、
前記第１の材料及び前記トレンチ充填酸化物に対して選択的に前記ポリシリコンから成る層を前記基板からエッチングする工程とを備える基板分離トレンチを形成するための半導体処理方法。
【請求項１０】　請求項９の基板分離トレンチを形成するための半導体処理方法において、前記突出するピラーをエッチングする工程が、前記ポリシリコンから成る層の下方の高さまで前記ピラーを下方にエッチングする段階を含むことを特徴とする基板分離トレンチを形成するための半導体処理方法。
【請求項１１】　基板分離トレンチを形成するための半導体処理方法において、
第１の選択された厚みを有し、酸化物から成る第１の層を基板の上に設ける工程と、
第３の選択された厚みを有し、酸化物に対して選択的にエッチング可能な選択されたエッチストップ材料から成る犠牲層をポリシリコンから成る前記酸化物層の上に設ける工程と、
前記犠牲層及び前記酸化物から成る層を通して前記基板の中へパターニング並びにエッチングを行い、分離トレンチを形成する工程と、
前記トレンチの中にトレンチをコーティングする絶縁層を設ける工程と、
前記エッチストップ材料に対して選択的にエッチング可能なポリシリコンから成る層を前記基板の上方に第４の選択された厚みまで堆積させると共に、前記分離トレンチの中に堆積させて該分離トレンチを充填する工程と、
平坦化エッチングを行うための効果的なエッチストップとして前記犠牲層を用い、前記トレンチ充填ポリシリコンを平坦化エッチングする工程と、
前記トレンチ充填ポリシリコン及び前記酸化物から成る第１の層に対して選択的に前記犠牲層を前記基板からエッチングし、これにより、酸化物から成る前記第１の層に対して相対的に上方へ突出するポリシリコンのピラーを残す工程と、
前記突出するピラーを前記酸化物から成る第１の層に対して選択的にエッチングする工程とを備える基板分離トレンチを形成するための半導体処理方法。

【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、半導体処理におけるトレンチ分離方法に関する。
【０００２】
【従来の技術】集積回路は、基板の領域をパターニングし且つ基板上の層をパターニングすることによって、シリコンウエーハ等の基板に化学的及び物理的に集積される。上記領域及び層を伝導性とし、導体及び抵抗を製造することができる。また、上記領域及び層に異なったタイプの伝導性をもたせることができ、これはトランジスタ及びダイオードの製造に必須の要件である。基板の中に種々の回路素子すなわちデバイスを形成する時には、そのようなデバイスを互いに分離すなわち絶縁することが必要となる。
【０００３】集積回路を製造する際に、バルク基板の中に形成されたデバイスを電気的に絶縁するための種々の技術が開発されてきた。開発されたある周知の技術は、シリコンの部分的な酸化（ＬＯｃａｌ　Ｏｘｉｄａｔｉｏｎ　ｏｆ　Ｓｉｌｉｃｏｎ）を略してＬＯＣＯＳ分離と呼ばれており、この技術においては、基板のノンアクティブ（又はフィールド）領域に半凹所型の酸化物を形成する。ＬＯＣＯＳ法の原理は、所望のフィールド領域に酸化物を選択的に成長させることである。このような酸化物の成長は、アクティブ領域を窒化ケイ素の薄い層で覆うことによって行われ、上記窒化ケイ素の薄い層はその下で酸化が起こるのを防止する。窒化物の層はパターニング及びエッチングされ、その中にフィールド酸化物が必要とされるシリコン領域を上方に露出させて成長させる。その後、ウエーハを酸化条件に露呈する。マスキング窒化物のない部分には酸化体が成長する。しかしながら、窒化物のマスキングの周縁部においては、幾分かの酸化物が側方に拡散する。
【０００４】これにより、窒化物の周縁部の下で酸化物が成長し、該周縁部を持ち上げる。窒化物の周縁部の酸化物の形状は、緩やかに傾斜する酸化物のクサビを形成し、このクサビは下層のパッドの酸化物層に合流する。上記クサビは鳥の嘴（ｂｉｒｄ’ｓ　ｂｅａｋ）と呼ばれている。鳥の嘴はフィールド酸化物の側方に伸長し、デバイスのアクティブ領域に入る。そのような分離技術の欠点の１つは、上記鳥の嘴が、窒化物にマスク開口を形成するために用いられる写真機能の最小寸法よりも大きな横方向の寸法を有するフィールド酸化物を生ずることである。
【０００５】従って、デバイスの幾何学的な形状がサブミクロンの寸法に近づくに連れ、通常のＬＯＣＯＳ分離

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技術の有効性はその限界に近づき、ＣＭＯＳ及びバイポーラ技術用の代替的な分離プロセスが必要とされている。そのような技術の１つとしてトレンチ分離がある。この技術においては、充填されて分離されたトレンチは、基板の中で垂直方向に配列され、該トレンチの両側にある電気デバイスを分離すなわち絶縁する。本発明は、上述の如き基板分離トレンチを形成するための処理方法に関するものである。

【０００６】従来技術のある分離トレンチ技術並びにその技術に伴う問題点を図１乃至図５を参照して説明する。図１は、バルク基板１２と、パッド酸化物の薄い層１４と、ホトレジストの層１６とから構成される半導体基板１０を示している。ホトレジスト層１６はパターニングされて接触開口２０を形成しており、該開口にはこれを貫通するトレンチが形成されることになる。

【０００７】図２を参照すると、パッド酸化物層１４及びバルク基板１２が図示のようにエッチングされ、空所すなわちトレンチ２２を形成している。

【０００８】図３を参照すると、SiO_2の層２４がトレンチ２２の中で成長している。

【０００９】図示のように、追加の分離インプラント２６をトレンチ２２の基部に設けることもできる。例えば、バルク基板１２が、ｎチャンネルのデバイスが設けられることになる（ｐ－）シリコンから構成される場合には、インプラント２６を（ｐ＋）インプラントとし、トレンチ２２の両側に形成されるべき回路要素の間に電気的な分離効果すなわち絶縁効果を更にもたらすことができる。そのインプラントは一般に、図１に示すマスク層を除去する前に設けられる。

【００１０】図４を参照すると、トレンチ充填材料から成る層２８がウエーハの頂部に設けられてトレンチ２２を充填している。層２８の材料は、トレンチ２２の容積を充填する嵩を有するポリシリコン又は酸化物、あるいは他の材料とすることができる。層２８の材料は必ずしも絶縁材料とする必要はない。その理由は、酸化物の層２６が、トレンチ２２の側方の領域に電気的な絶縁効果をもたらすからである。そのような層は一般に等角状に堆積され、図示のような凹所すなわちＶ字型の部分３０を形成する。

【００１１】図５を参照すると、層２８は適宜なエッチングに露呈され、概ね充填されたトレンチ２２を残す点まで除去される。しかしながら、層２８の等角状に堆積する性質により、一般にはエッチングの後にも図示のようにＶ字型の部分３０ａが残ってしまい、これは望ましくない。

【００１２】

【発明が解決しようとする課題】基板分離トレンチを形成する上述の技術及び他の技術を改善することが望ましい。

【００１３】

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【課題を解決するための手段】本発明のある特徴によれば、基板分離トレンチを形成するための半導体処理方法は、選択された厚みを有し、選択された材料から成る層を基板の上に設ける工程と、選択された厚みを有し、選択されたエッチストップ材料から成る犠牲層を上記選択された材料から成る層の上に設ける工程と、上記犠牲層及び上記選択された材料から成る層を通して上記基板の中へパターニング並びにエッチングを行い、分離トレンチを形成する工程と、選択された厚みを有するトレンチ充填材料を上記基板の上方並びに上記分離トレンチの中に堆積させ、上記分離トレンチを充填する工程と、平坦化エッチングを行うための効果的なエッチストップとして上記犠牲層を用い、上記トレンチ充填材料を平坦化エッチングする工程と、上記基板から上記犠牲層をエッチングし、これにより、基板の上面に対して相対的に上方へ突出するトレンチ充填材料のピラーを残す工程と、上記突出するピラーを上記基板の上面に対して選択的にエッチングする工程とを備える。

【００１４】更に詳細に言えば、本発明の別の特徴によれば、基板分離トレンチを形成するための方法は、第１の選択された厚みを有し、第１の材料から成る層を基板の上に設ける工程と、第２の選択された厚みを有し、ポリシリコンから成る層を上記基板の上方に設ける工程と、第３の選択された厚みを有し、ポリシリコンに対して選択的にエッチング可能な選択されたエッチストップ材料から成る犠牲層を上記ポリシリコンから成る層の上に設ける工程と、上記犠牲層、上記ポリシリコンから成る層、及び上記第１の材料から成る層を通して上記基板の中へパターニング並びにエッチングを行い、分離トレンチを形成する工程と、上記エッチストップ材料に対して選択的にエッチング可能な酸化物から成る層を上記基板の上方に第４の選択された厚みまで堆積させると共に、上記分離トレンチの中に堆積させて該分離トレンチを充填する工程と、平坦化エッチングを行うための効果的なエッチストップとして上記犠牲層を用い、上記トレンチ充填材料を平坦化エッチングする工程と、上記トレンチ充填酸化物及び上記ポリシリコンから成る層に対して選択的に上記犠牲層を上記基板からエッチングし、これにより、ポリシリコンから成る層に対して相対的に上方へ突出する酸化物のピラーを残す工程と、上記突出するピラーを上記ポリシリコンから成る層に対して選択的にエッチングする工程と、上記第１の材料及び上記トレンチ充填酸化物に対して選択的に上記ポリシリコンから成る層を上記基板からエッチングする工程とを備える。

【００１５】本発明の更に別の特徴によれば、基板分離トレンチを形成するための方法は、第１の選択された厚みを有し、酸化物から成る第１の層を基板の上に設ける工程と、第３の選択された厚みを有し、酸化物に対して選択的にエッチング可能な選択されたエッチストップ材料から成る犠牲層をポリシリコンから成る上記酸化物層

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の上に設ける工程と、上記犠牲層及び上記酸化物から成る層を通して上記基板の中へパターニング並びにエッチングを行い、分離トレンチを形成する工程と、上記トレンチの中にトレンチをコーティングする絶縁層を設ける工程と、上記エッチストップ材料に対して選択的にエッチング可能なポリシリコンから成る層を上記基板の上方に第４の選択された厚みまで堆積させると共に、上記分離トレンチの中に堆積させて該分離トレンチを充填する工程と、平坦化エッチングを行うための効果的なエッチストップとして上記犠牲層を用い、上記トレンチ充填ポリシリコンを平坦化エッチングする工程と、上記トレンチ充填ポリシリコン及び上記酸化物から成る第１の層に対して選択的に上記犠牲層を上記基板からエッチングし、これにより、酸化物から成る上記第１の層に対して相対的に上方へ突出するポリシリコンのピラーを残す工程と、上記突出するピラーを上記酸化物から成る第１の層に対して選択的にエッチングする工程とを備える。

【００１６】

【実施例】以下に図面を参照して本発明の好ましい実施例を説明する。

【００１７】図６乃至図１３を参照してより詳細に説明すれば、本発明のある処理工程にある半導体基板の全体が参照符号３０で示されており、この半導体基板の一部は大きな基板材料すなわちバルク基板３２から構成されている。一般にバルク基板３２は、軽度な導電性のドーピング処理を受けたシリコン（すなわち、ドーパント濃度が2×10^{15}原子／cm^3）から構成されるのが好ましい。第１の材料層３４が、第１の選択された厚みを有するようにバルク基板３２の頂部に設けられる。この実施例の層３４は、熱成長すなわち蒸着されたSiO_2等の酸化物から構成されるのが好ましい。上記第１の選択された厚みは、約１００オングストロームから約５００オングストロームであるのが好ましい。

【００１８】第２の材料層３６が、第２の選択された厚みを有するように基板の上方で層３４の上に設けられる。第２の材料層３６は、第１の材料層３４に対して選択的にエッチング可能である。一例として、好ましい材料はポリシリコンであり、上記第２の選択された厚みは、約１００オングストロームから約１０００オングストロームであるのが好ましい。以下の記載においては、層３６が基板の上面３７を画成するものとして説明する。

【００１９】選択されたエッチストップ（エッチング停止）材料から成る犠牲層３８が、第３の選択された厚みを有するように基板の上方で第２の材料層３６の上に設けられる。エッチストップ材料は、第２の材料に対して選択的にエッチング可能であり、Si_3N_4の如き窒化物から構成されるのが好ましい。上記第３の選択された厚みは、約５００オングストロームから約３０００オングストロームであるのが好ましい。

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【００２０】図７を参照すると、犠牲層３８、第２の材料層３６、第１の材料層３４及びバルク基板３２がパターニングされ且つ順次エッチングされて分離トレンチ４０を形成している。必要であれば、図３に示す従来技術のインプラント２６と同様な分離インプラントをトレンチ４０の基部に設けることができる。

【００２１】図８を参照すると、トレンチ充填材料層４２が、第４の選択された厚みを有するように基板の上方に堆積されると共に、分離トレンチ４０の内部を充填している。トレンチ充填材料は、第２の材料に対して選択的にエッチング可能であり、また、第２の材料もトレンチ充填材料に対して選択的にエッチング可能である。また、エッチストップ材料は、トレンチ充填材料に対して選択的にエッチング可能である。この実施例における好ましいトレンチ充填材料の例は、SiO_2の如き酸化物である。そのような酸化物は、ＴＥＯＳ蒸着の如き周知の技術によって堆積させることができ、また、必要に応じてホウ素及び／又はリンでドーピングすることができる。上記第４の選択された厚みは、トレンチの寸法に応じて、約２０００オングストロームから約３０００オングストロームであるのが好ましい。例えば、トレンチが浅くなると、好ましい第４の選択された厚みも薄くなる。

【００２２】図９を参照すると、犠牲層３８を平坦化エッチングのための効果的なエッチストップとして用いて、層４２に平坦化エッチング技術が施されている。本発明における極めて好ましい平坦化エッチング技術は、化学機械的な研磨（ＣＭＰ）である。層４２が酸化物から構成され、また、層３８が窒化物から構成される場合のＣＭＰスラリの例は、ＫＯＨ中に摩耗性のSiO_2を含むスラリである。そのようなスラリは、１分間当たり０．３ミクロンのエッチング速度をもたらし、図９に示す構造を形成する。

【００２３】図１０を参照すると、犠牲層３８が、第２の材料層３６及びトレンチ充填材料４２に対して相対的に、基板から選択的にエッチングされ、第２の材料層３６から上方に突出するトレンチ充填材料のピラー４４が残されている。このようにして、犠牲層３８が基板からエッチングされ、表面３７の如き基板の上面に対して相対的に上方へ突出するトレンチ充填材料のピラーが形成される。

【００２４】図１１を参照すると、突出するピラー４４が、第２の材料層３６に対して相対的に、またこれに対応して基板の上面３７に対して相対的に選択的にエッチングされ、トレンチ４０の中には材料４２が残っている。図示のように、そのようなエッチングは、第２の材料層３６の直ぐ下方で且つシリコン基板材料３２の上面よりも高いすなわち上方の高さまで、ピラー４４をエッチングすることにより実行するのが好ましい。

【００２５】図１２を参照すると、第２の材料層３６

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が、第１の材料層３４及びトレンチ充填材料に対して相対的に、基板から選択的にエッチングされている。層３６がポリシリコンから構成される場合のエッチング条件の例は、酸化物に対して優れた選択性を示す湿式ポリシリコンＨＦ／ＨＮＯ，／Ｈ，Ｏの化学作用を利用することである。

【００２６】図１３を参照すると、層３４及びこれに対応する等しい厚みのトレンチ材料４２がエッチングされ、図示のような分離トレンチ４０がもたらされている。

【００２７】本発明の代替的なプロセスが図１４乃至図１９に示されている。適正な範囲で、図６乃至図１３の実施例の層の参照符号と同じ参照符号を用いている。図１４は、トレンチ４０が形成されている代替的な基板３０ａを示している。図１４の実施例が図７に示す第１の実施例と異なる点は、図７の層３６の如きポリシリコン層が何等設けられていないことである。他の層は、図６乃至図１３の実施例に示される通りである。必要であれば、図３に示す従来技術のインプラントと同様な分離インプラントをトレンチ４０の基部に設けることができる。

【００２８】図１５を参照すると、絶縁材料製のトレンチコーティング５０が、トレンチ４０の側壁の内側並びにトレンチの側壁及び基部の周囲に設けられている。トレンチコーティング５０は、基板３０ａを酸化条件に露呈させることにより成長させるすなわち設けることができる。

【００２９】図１６を参照すると、ポリシリコンから形成されるのが好ましいトレンチ充填材料の層４２ａが、第４の選択された厚みまで堆積されている。層４２ａは、この実施例においては、シリコンのバルク基板３２と同一の主要な材料から形成されるポリシリコンで構成されているので、絶縁すなわち分離する材料のトレンチコーティング５０を設け、バルク基板３２（シリコン）がトレンチ４０の中のポリシリコン材料４２ａに接触するのを防止している。

【００３０】図１７を参照すると、層４２ａは平坦化エッチングを受けており、このエッチングは、そのような平坦化エッチングに対する有効なエッチストップとしてエッチストップ層３８を用いて、ＣＭＰによって行うのが好ましい。

【００３１】図１８を参照すると、犠牲層３８は、トレンチ充填ポリシリコン及び第１の酸化物層３４に対して相対的に、基板から選択的にエッチングされ、材料４２ａから成る突出したピラー４４を残している。

【００３２】図１９を参照すると、突出するピラー４４が、第１の酸化物層３４に対して相対的に選択的にエッチングされている。この代替実施例は、追加の層３６を堆積させる必要性を排除し且つトレンチコーティング層５０をもたらすことに注意する必要がある。必要に応じて、その後層３４及びこれに等しい材料４２ａの厚みをウエーハからエッチングすることができる。

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【００３３】上述の技術は従来技術よりも優れた効果をもたらし、特に、シリコンの表面／トレンチの縁部と同一平面にある比較的平坦なトレンチ充填材料を提供する。トレンチエッチと組み合わせて本発明のエッチストップ材料を用いることは、新規且つ非自明であり、その理由は、上記エッチストップ材料の使用により、その後トランジスタが形成されるシリコン表面に悪影響を与えることなく、ＣＭＰ又は他の平坦化エッチングの後にトレンチ充填材料のエッチバックを可能とするからである。

【００３４】

【発明の効果】本発明によれば、優れた基板分離トレンチを形成できる。

【図面の簡単な説明】

【図１】従来の技術の項で説明した従来技術の方法に従って処理された半導体ウエーハの断片の概略的な断面図である。

【図２】図１に示す処理工程の次の従来技術の処理工程にある図１のウエーハを示す断面図である。

【図３】図２に示す処理工程の次の従来技術の処理工程にある図１のウエーハを示す断面図である。

【図４】図３に示す処理工程の次の従来技術の処理工程にある図１のウエーハを示す断面図である。

【図５】図４に示す処理工程の次の従来技術の処理工程にある図１のウエーハを示す断面図である。

【図６】本発明のある処理工程にある半導体ウエーハの断片を示す概略的な断面図である。

【図７】図６に示す処理工程の次の処理工程にある図６のウエーハを示す断面図である。

【図８】図７に示す処理工程の次の処理工程にある図６のウエーハを示す断面図である。

【図９】図８に示す処理工程の次の処理工程にある図６のウエーハを示す断面図である。

【図１０】図９に示す処理工程の次の処理工程にある図６のウエーハを示す断面図である。

【図１１】図１０に示す処理工程の次の処理工程にある図６のウエーハを示す断面図である。

【図１２】図１１に示す処理工程の次の処理工程にある図６のウエーハを示す断面図である。

【図１３】図１２に示す処理工程の次の処理工程にある図６のウエーハを示す断面図である。

【図１４】本発明の代替的な方法のある処理工程にある半導体ウエーハの断片の概略的な断面図である。

【図１５】図１４に示す処理工程の次の処理工程にある図１４のウエーハを示す断面図である。

【図１６】図１５に示す処理工程の次の処理工程にある図１４のウエーハを示す断面図である。

【図１７】図１６に示す処理工程の次の処理工程にある

図１４のウエーハを示す断面図である。

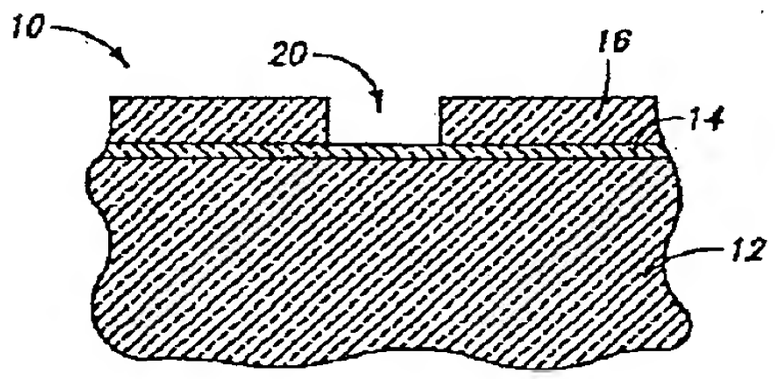
【図１８】図１７に示す処理工程の次の処理工程にある図１４のウエーハを示す断面図である。

【図１９】図１８に示す処理工程の次の処理工程にある図１４のウエーハを示す断面図である。

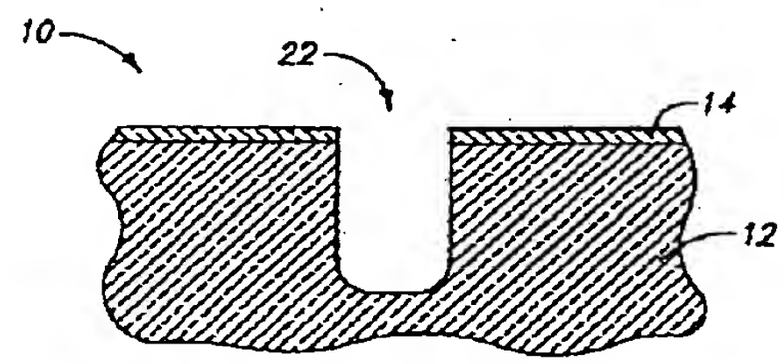
【符号の説明】

３０　半導体基板　　３２　バルク基板
３４　第１の材料層　　３６　第２の材料層
３７　基板の上面　　３８　犠牲層
４０　トレンチ　　４２　トレンチ充填材料
４２　トレンチ充填材料層　　４４　ピラー
５０　トレンチコーティング

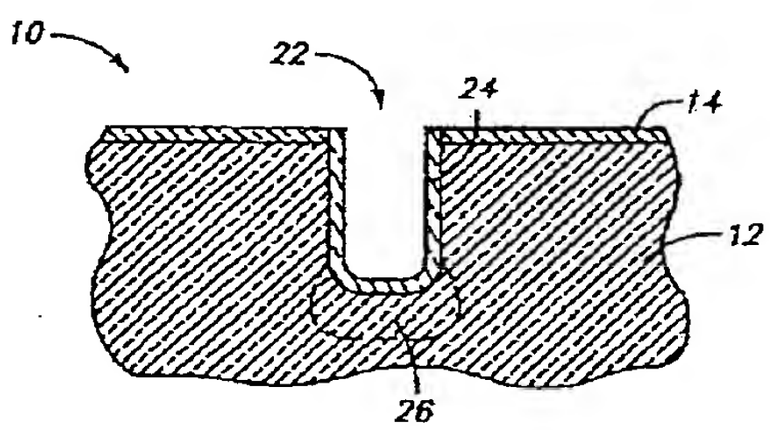
【図１】



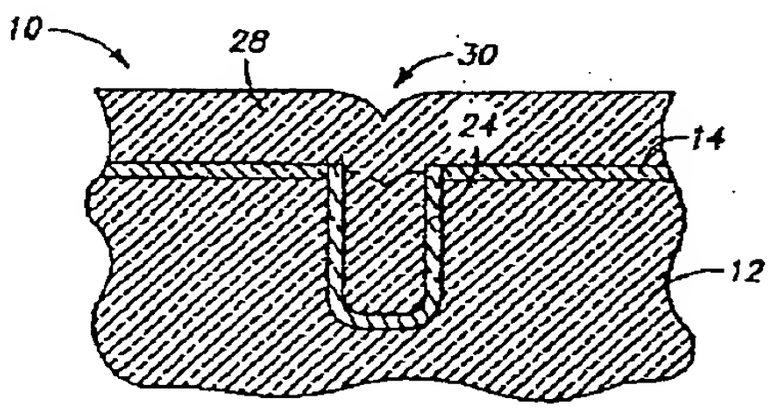
【図２】



【図３】



【図４】



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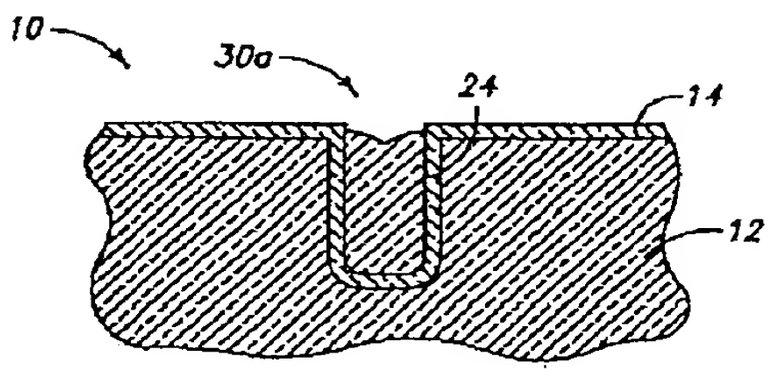
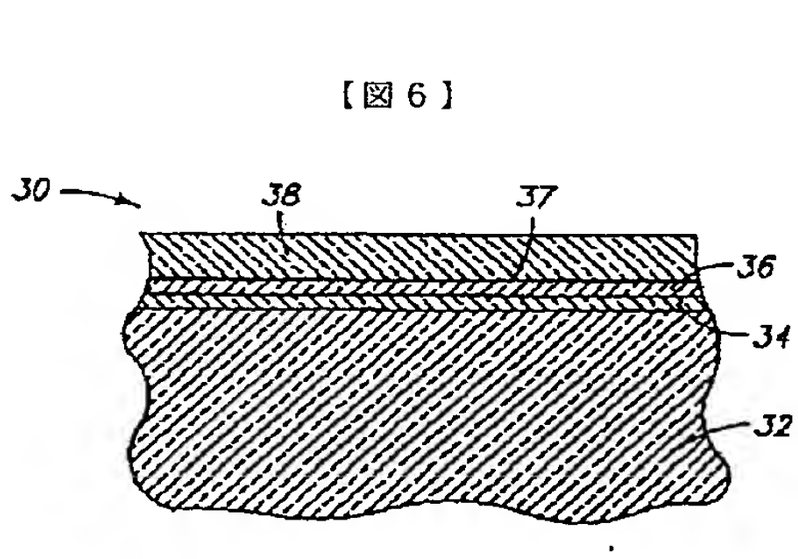
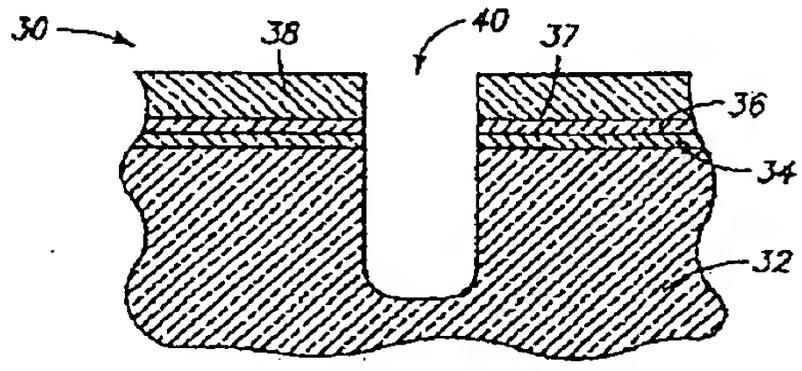


【図６】



【図７】



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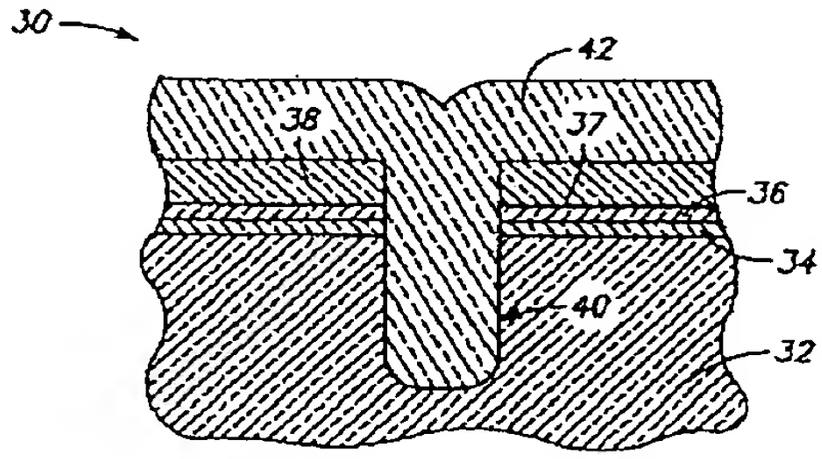

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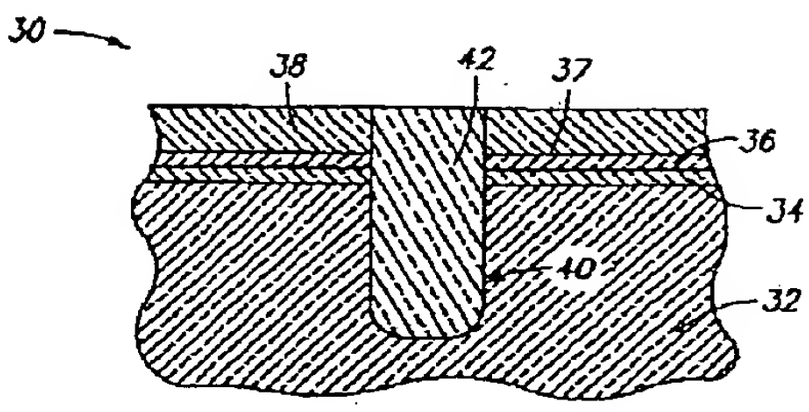
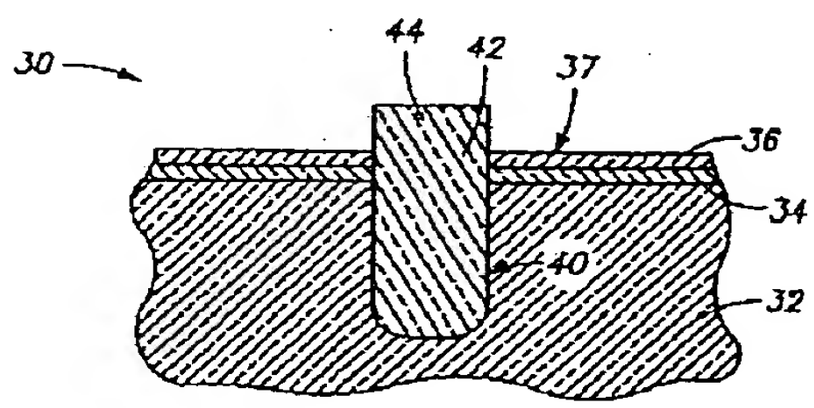
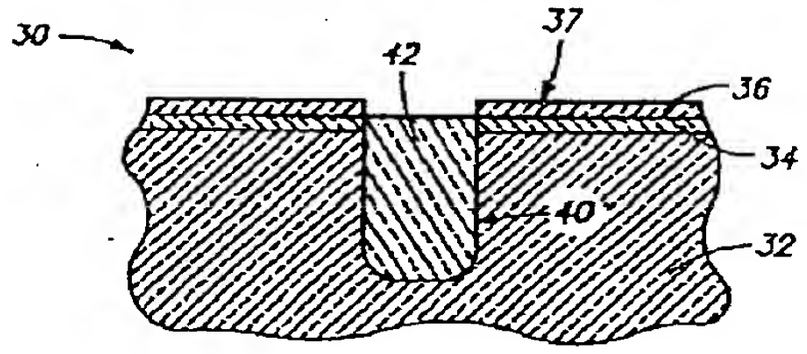


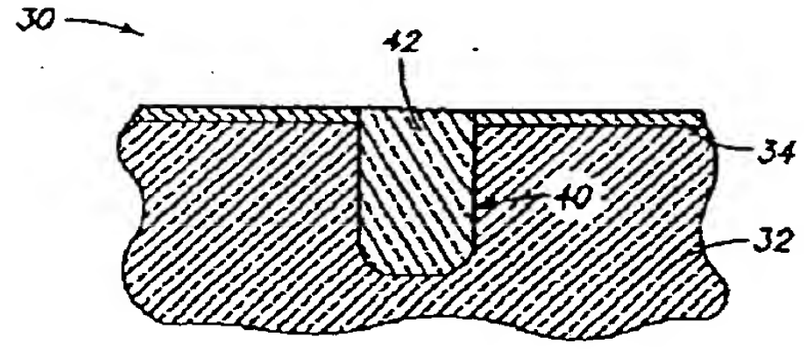
【図１０】



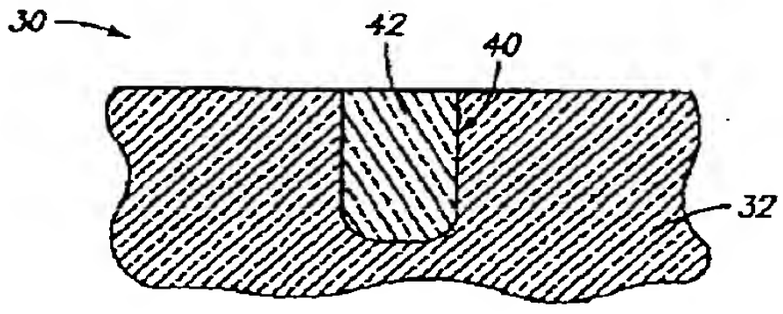
【図１１】



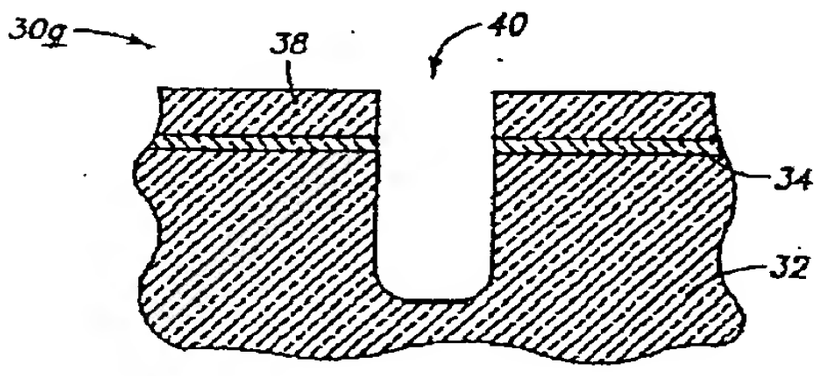
【図１２】



【図１３】



【図１４】



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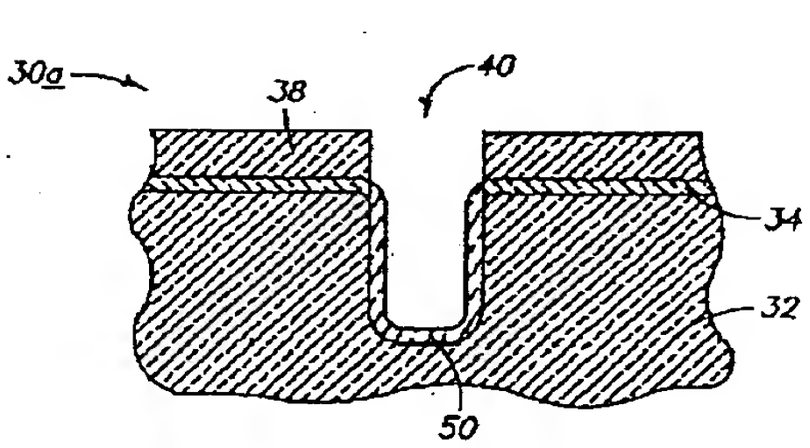
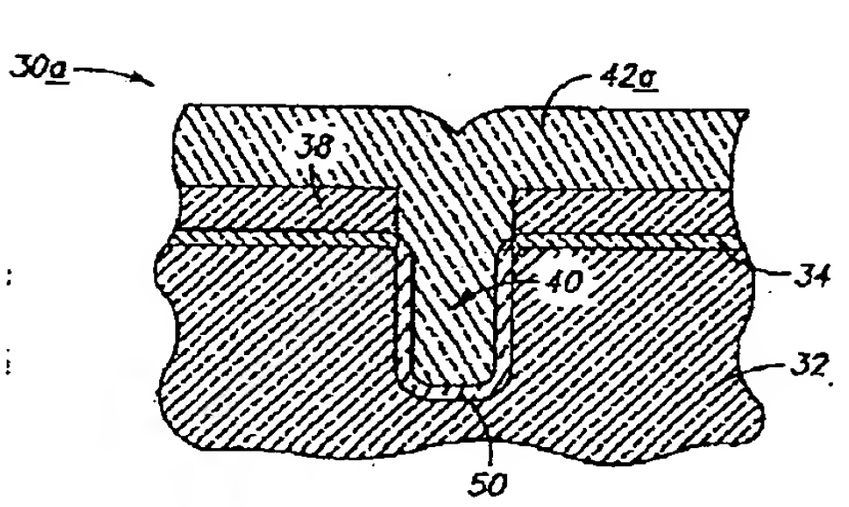
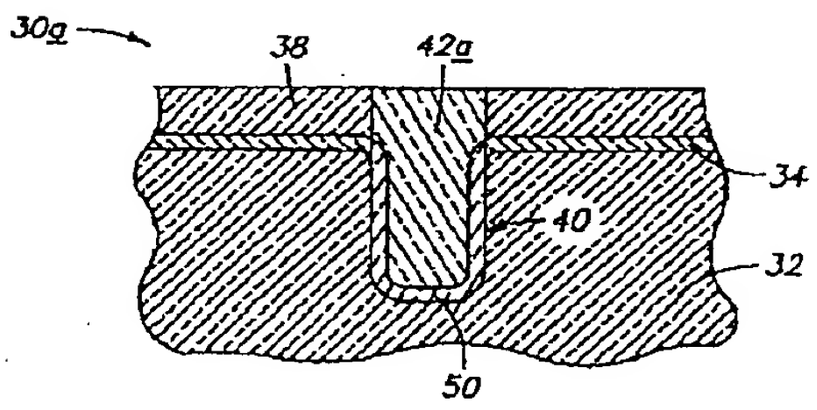


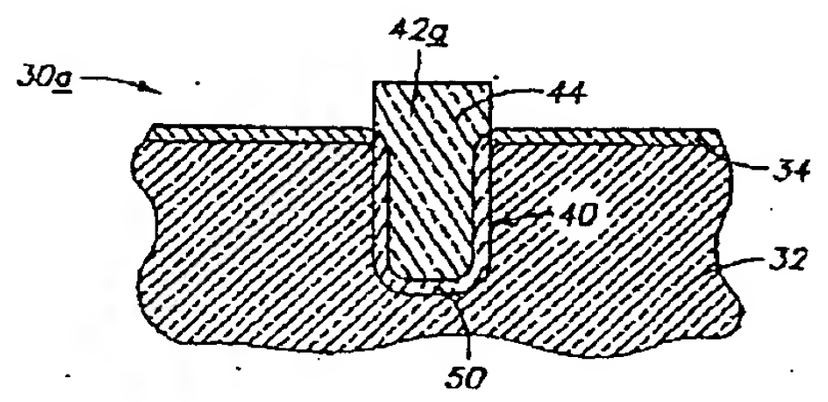
【図１６】



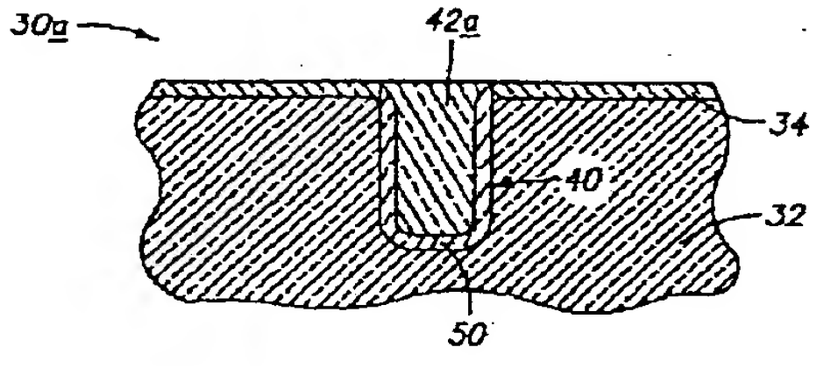
【図１７】



【図１８】



【図１９】



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